

< DIIPM >

Mini DIIPM with BSD Series APPLICATION NOTE

PSS**S51F6 / PSS**S71F6

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CHAPTER 1 INTRODUCTION

1.1 Features of Mini DIIPM with BSD

Mini DIIPM with BSD is an ultra-small compact intelligent power module with transfer mold package favorable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which make it easy for AC100-240V class low power motor inverter control. This series is developed as a succession model of current Mini DIIPM Ver.3 (5~20A/600V) and Ver.4 series (20,30A/600V) with 2500Vrms isolation voltage. It includes many improvements (loss performance, built-in peripheral functions and line-up expansion). Main features of this series are as below.

- **Newly developed 6th generation CSTBT are integrated for improving efficiency**
- **Expanding the line-up to 50A (Current products are up to 30A)**
- **Incorporating bootstrap diode(BSD) with current limiting resistor for P-side gate driving supply**
- **Newly integrated temperature of control IC part output function**
- **Same package with current Ver.3 and Ver.4. (A part of terminal shape and assignment are different.)**

About detailed differences, please refer Section 1.5. Fig.1-1-1 and Fig.1-1-2 show the outline and internal cross-section structure respectively.

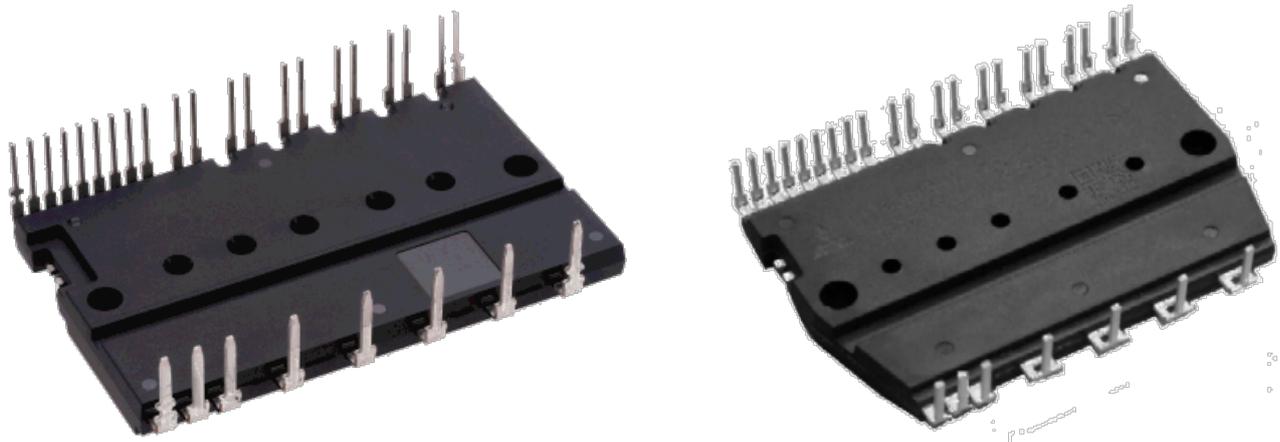


Fig.1-1-1 Package image Left: 20~50A products Right: 5~20A products

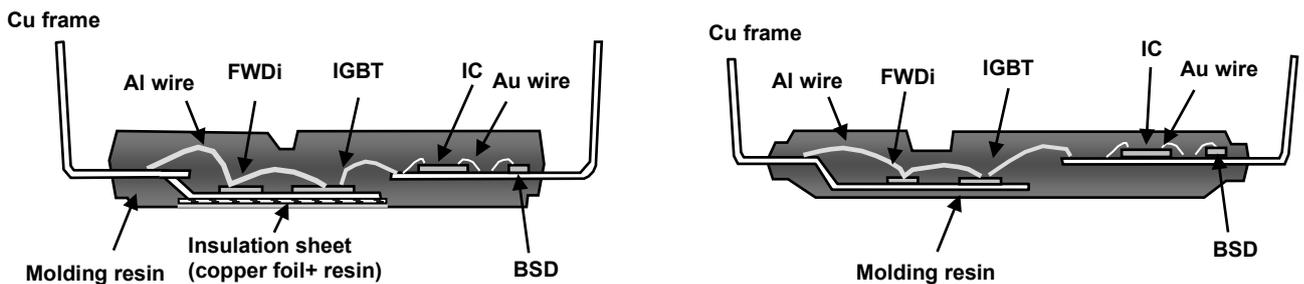


Fig.1-1-2 Internal cross-section structure Left: 20~50A products Right: 5~20A products

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1.2 Functions

Mini DIIPM has following functions and inner block diagram is described in Fig.1-2-1.

- For P-side IGBTs:
 - Drive circuit;
 - High voltage level shift circuit;
 - Control supply under voltage (UV) lockout circuit (without fault signal output).
 - Built-in bootstrap diode (BSD) with current limiting resistor
- For N-side IGBTs:
 - Drive circuit;
 - Short circuit (SC) protection circuit (by inserting external shunt resistor into main current path)
 - Control supply under voltage (UV) lockout circuit (with fault signal output)
 - Outputting LVIC temperature by analog signal (No self over temperature protection)
- Fault Signal Output
 - Corresponding to N-side IGBT SC and N-side UV protection.
- IGBT Drive Supply
 - Single DC15V power supply (in the case of using bootstrap method)
- Control Input Interface
 - Schmitt-triggered 3V, 5V input compatible, high active logic.
- UL recognized : UL1557 File E80276
-

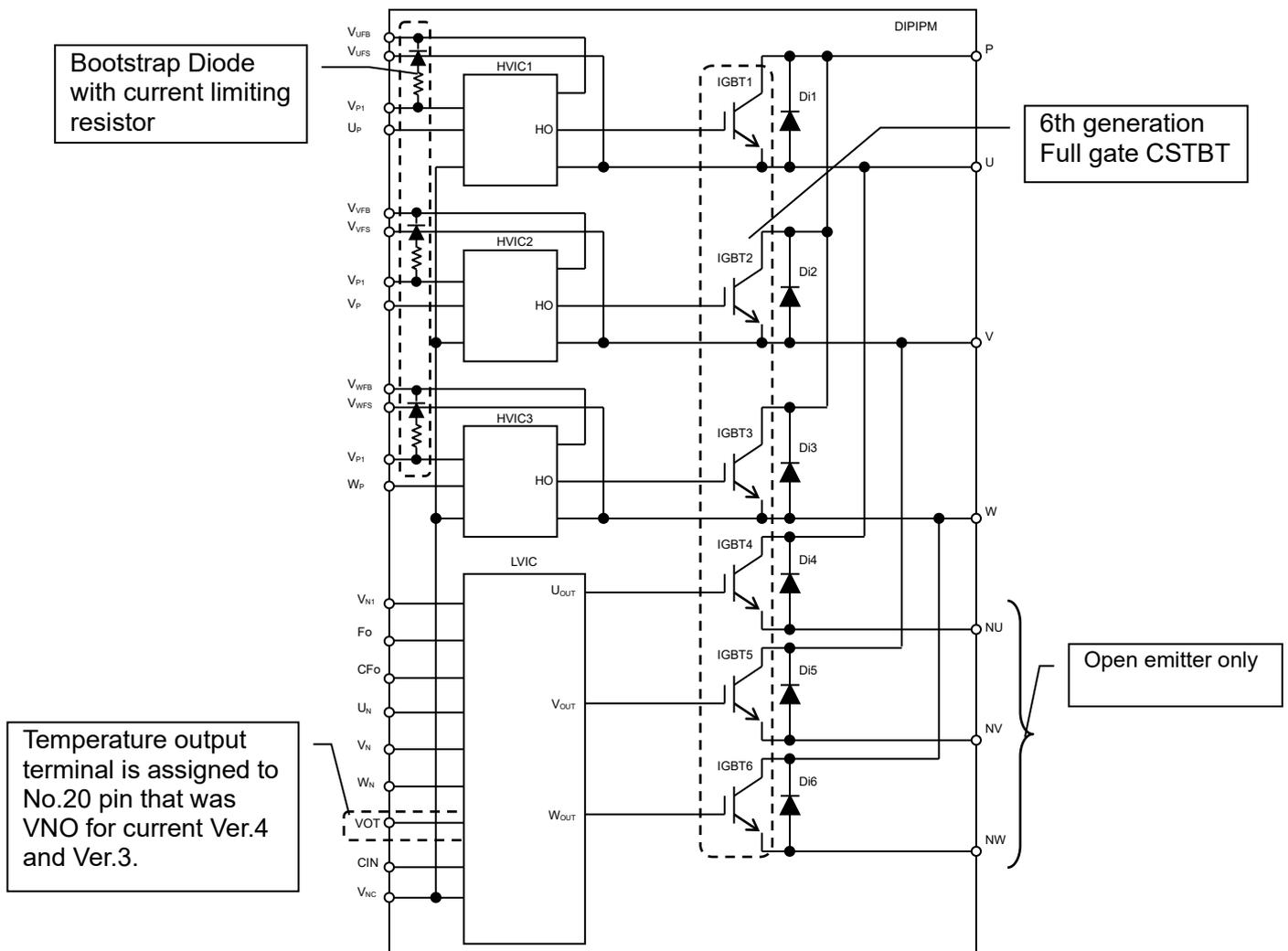


Fig.1-2-1 Inner block diagram

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1.3 Target Applications

Motor drives for low power industrial equipment and household equipment such as air conditioners, hot water system and so on. (Except for vehicle application)

1.4 Product Line-up

Table 1-4-1 Mini DIIPM Line-up (Mini DIP Ver.3 package)

Type Name (Note 1)	IGBT Rating	Motor Rating (Note 2)	Isolation Voltage
PSS05S51F6/-C	5A/600V	0.2kW	V _{iso} = 2500Vrms (Sine 60Hz, 1min) All shorted pins-heat sink)
PSS10S51F6/-C	10A/600V	0.4kW	
PSS15S51F6/-C	15A/600V	0.75kW	
PSS20S51F6/-C	20A/600V	1.5kW	

Table 1-4-2 Mini DIIPM Line-up (Mini DIP Ver.4 package)

Type Name (Note 1)	IGBT Rating	Motor Rating (Note 2)	Isolation Voltage
PSS20S71F6	20A/600V	1.5kW	V _{iso} = 2500Vrms (Sine 60Hz, 1min) All shorted pins-heat sink)
PSS30S71F6	30A/600V	2.2kW	
PSS50S71F6	50A/600V	3.7kW	

Note 1: PSSxxS51F6 has two terminal shapes. 'C' indicates control terminal zigzag pin type. Please refer to chapter 2 for details.

Note 2: The motor ratings are calculation results. It will depend on the operation conditions.

1.5 The Differences between Previous Series and This Series

Mini DIIPM has some differences against current Mini DIP Ver.3 (PS2156x) or Ver.4 (PS2176x)

Main differences are described in Table 1-5-1 and Table 1-5-2.

Table 1-5-1 Differences of functions and outlines

Items	PS2156x	PSSxxS51F6	PS2176x	PSSxxS71F6	Ref.
Package	Mini Ver.3	Same with Ver.3 ³⁾	Mini Ver.4	Same with Ver.4	
Bootstrap diodes	None	Built-in	None	Built-in	Section 4.2
V _{OT} output (LVIC temp. output)	None	Built-in ¹⁾	None	Built-in ¹⁾	Section 2.2.4
No.20 terminal	VNO or NC	V _{OT} ²⁾	VNO	V _{OT} ²⁾	Section 2.3.3
N-side IGBT emitter terminal	Common / Open	Open ³⁾	Open	Open	Section 2.3
Terminal shapes	Short(1shunt), Short(3 shunts)	Short Control terminal side zig-zag	Short	Short	Section 2.3

(1) V_{OT} function cannot shutdown by itself when LVIC temperature exceeds protection level. So it is necessary for system controller to monitor this V_{OT} output and shutdown when the temperature reaches the protection level.

(2) No.20 pin, which was assigned to VNO or NC for former products, is set as V_{OT} output for this series. If the current PCB which was designed for former products is used for this new product, it is necessary to change the wiring of the PCB.

(3) N-side IGBT emitter terminal is open emitter type only. Terminal shape of N-side IGBT emitter for PSSxxS51F6 is different from the shape of 3shunts type of former Mini DIP Ver.3 series (PS2156x-SP).

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Table 1-5-2 Differences of specifications and recommended operating conditions

Items	Symbol	PS2156x	PS2176x	PSSxxS51F6	PSSxxS71F6
		Mini Ver.3	Mini Ver.4	Ver.3 package	Ver.4 package
Circuit current for IC (Low voltage part)	I_D	Max. 7.0mA	Max. 7.0mA	Max. 6.0mA	Max. 6.0mA
Short circuit trip level	$V_{SC(ref)}$	0.45~0.52V	0.43~0.53V	0.45~0.51V	0.45~0.51V
Fault output pulse width ($C_{Fo}=22nF$)	t_{Fo}	Typ. 1.8ms	Typ. 1.8ms	Typ. 2.4ms	Typ. 2.4ms
Input current	I_{IN}	Max. 2.0mA	Max. 2.0mA	Max. 1.5mA	Max. 1.5mA
Inner pull down resistance of input terminal	-	Min. 2.5k Ω	Min. 2.5k Ω	Min. 3.3k Ω	Min. 3.3k Ω
Bootstrap Di forward voltage	V_F	-	-	Typ. 0.9V @10mA	Typ. 0.9V @10mA
Arm-shoot-through blocking time	t_{dead}	Min. 1.5 μ s	Min. 2.0 μ s	Min. 1.5 μ s	Min. 1.5 μ s Min. 2 μ s(50A)
Allowable minimum input pulse width	PWIN(on)	0.3 μ s	0.3 μ s	1.0 μ s	0.7 μ s
	PWIN(off)	Depend on current rating	Depend on current rating	1.0 μ s	Depend on current rating

For more detail and the other characteristics, please refer the datasheet or application note for each product.

CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Mini DIIPM with BSD Specifications

Mini DIIPM specifications are described below by using PSS20S71F6 (20A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PSS20S71F6 are shown in Table 2-1-1.

Table 2-1-1 Maximum Ratings

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU, NV, NW	500	V
V_{CES}	Collector-emitter voltage		600	V
$\pm I_c$	Each IGBT collector current	$T_C = 25^\circ\text{C}$ (Note)	20	A
$\pm I_{cP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$, less than 1ms	40	A
P_C	Collector dissipation	$T_C = 25^\circ\text{C}$, per 1 chip	76.9	W
T_J	Junction temperature		-20~+150	$^\circ\text{C}$

Note: Pulse width and period are limited due to junction temperature.

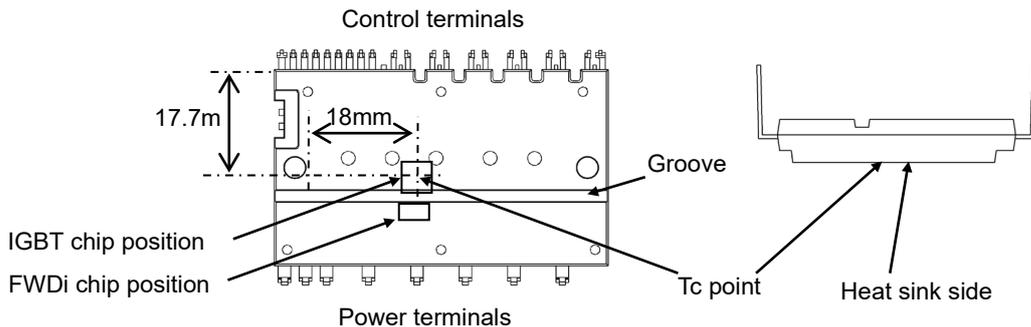
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between $V_{P1-V_{NC}}$, $V_{N1-V_{NC}}$	20	V
V_{DB}	Control supply voltage	Applied between $V_{UFB-V_{UFS}}$, $V_{VFB-V_{VFS}}$, $V_{WFB-V_{WFS}}$	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{NC} , U_N, V_N, W_N-V_{NC}	-0.5- $V_D+0.5$	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5- $V_D+0.5$	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between $C_{IN-V_{NC}}$	-0.5- $V_D+0.5$	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(prot)}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$, Inverter Part $T_J = 125^\circ\text{C}$, non-repetitive, less than 2 μs	400	V
T_C	Module case operation temperature	Measurement point of T_C is described below	-20~+100	$^\circ\text{C}$
T_{stg}	Storage temperature		-40~+125	$^\circ\text{C}$
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	V_{rms}

T_C measurement position



- (1) V_{CC} The maximum voltage can be biased between P-N. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.
- (2) $V_{CC(surge)}$ The maximum P-N surge voltage in switching state. If P-N voltage exceeds this voltage, a snubber circuit is necessary to absorb the surge under this voltage.
- (3) V_{CES} The maximum sustained collector-emitter voltage of built-in IGBT and FWDi.
- (4) $\pm I_c$ The allowable continuous current flowing at collect electrode ($T_C=25^\circ\text{C}$) Pulse width and period are limited due to junction temperature.
- (5) T_J The maximum junction temperature rating is 150°C . But for safe operation, it is recommended to limit the average junction temperature up to 125°C . Repetitive temperature variation ΔT_J affects the life time of power cycle, so refer life time curves for safety design.
- (6) $V_{CC(prot)}$ The maximum supply voltage for turning off IGBT safely in the case of an SC or OC faults. The power chip might not be protected and break down in the case that the supply voltage is higher than this specification.

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(7) T_c position T_c (case temperature) is defined to be the temperature just beneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest T_c point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip. About Ver.3 package type PSSxxS51F6, its surface of heat radiation part is molding resin surface, so operation temperature measuring point is defined at the heatsink temperature T_f under the power chip.

[Power chip position]

Fig.2-1-1,2 indicate the position of the each power chips. (This figure is the view from laser marked side.)

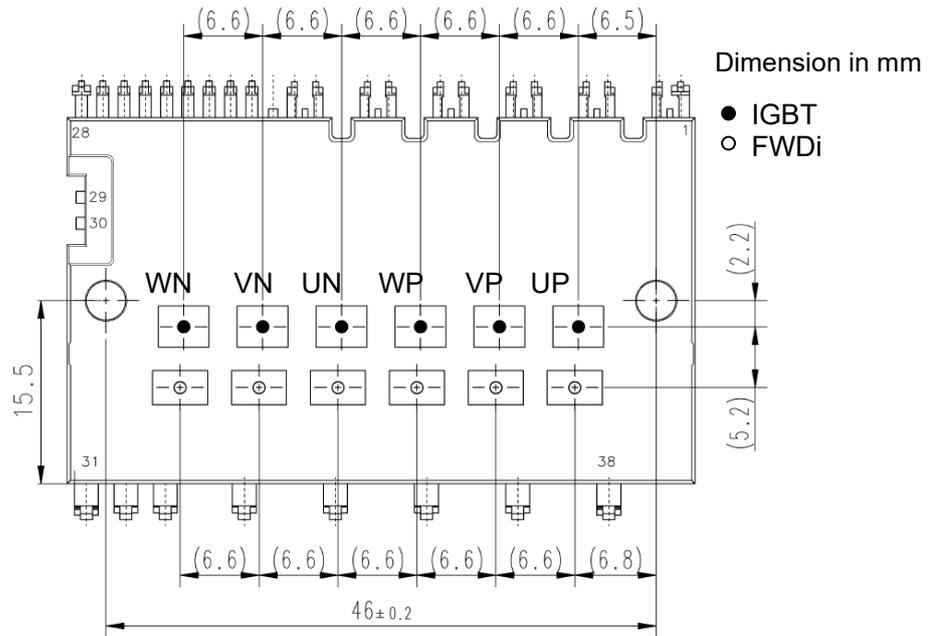


Fig.2-1-1 Power chip position (PSSxxS71F6)

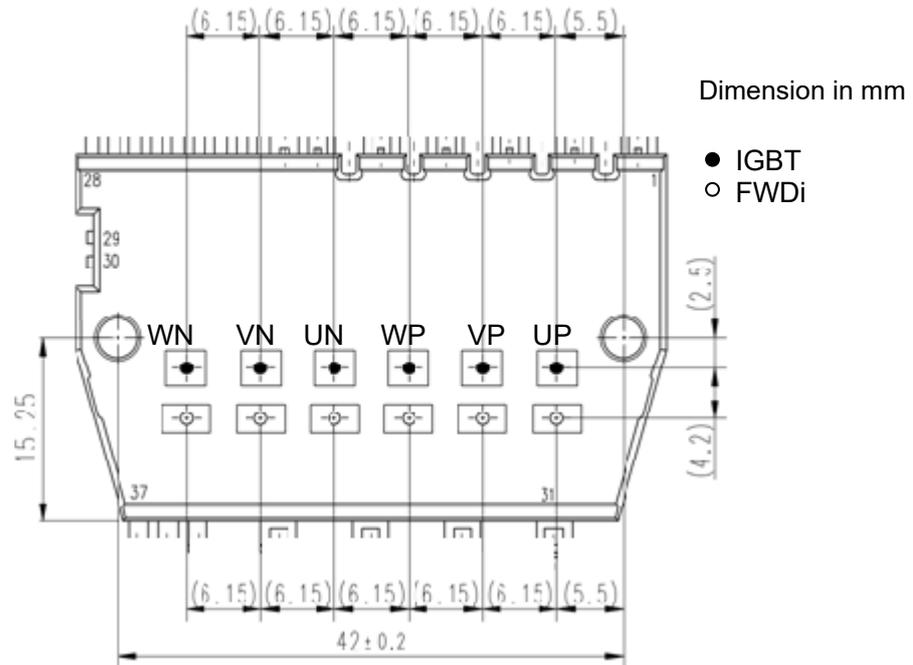


Fig.2-1-2 Power chip position (PSSxxS51F6)

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2.1.2 Thermal Resistance

Table 2-1-2 shows the thermal resistance of PSS20S71F6.

Table 2-1-2 Thermal resistance of PSS20S71F6

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note)	Inverter IGBT part (per 1/6 module)	-	-	1.3	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	3.0	K/W

Note : Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100 μ m~+200 μ m on the contacting surface of DIIPM and heat sink. The contacting thermal resistance between DIIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.3K/W (per 1/6 module, grease thickness: 20 μ m, thermal conductivity: 1.0W/m·k). The thermal resistance of PSSxxS51F6 is defined as the resistance between junction-heatsink ($R_{th(j-f)}$) which includes $R_{th(c-f)}$

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The unsaturated thermal resistance is called as transient thermal impedance which is shown in Fig.2-1-3. $Z_{th(j-c)}^*$ is the normalized value of the transient thermal impedance. ($Z_{th(j-c)}^* = Z_{th(j-c)} / R_{th(j-c)max}$)

For example, the IGBT transient thermal impedance of PSS20S71F6 in 0.2s is $1.3 \times 0.8 = 1.04K/W$.

The transient thermal impedance isn't used for constantly current, but for short period current (ms order). (e.g. in the cases at motor starting, at motor lock...)

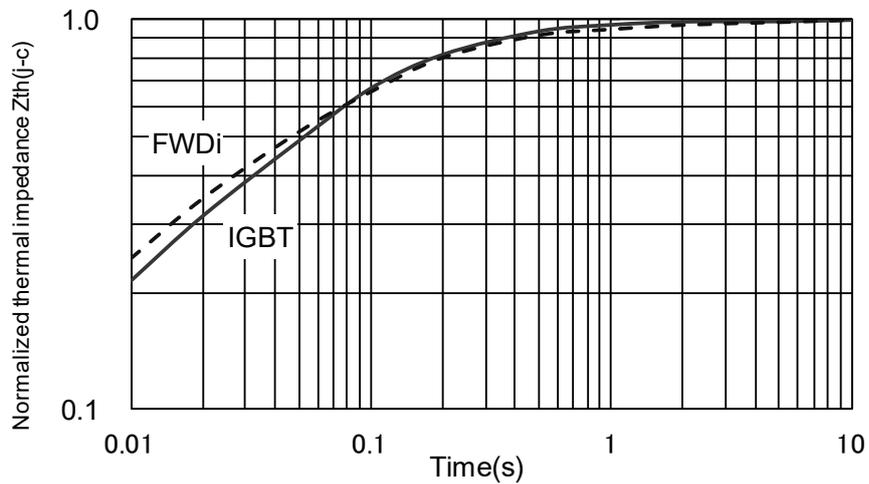


Fig.2-1-3 Typical transient thermal impedance (PSSxxS71F6)

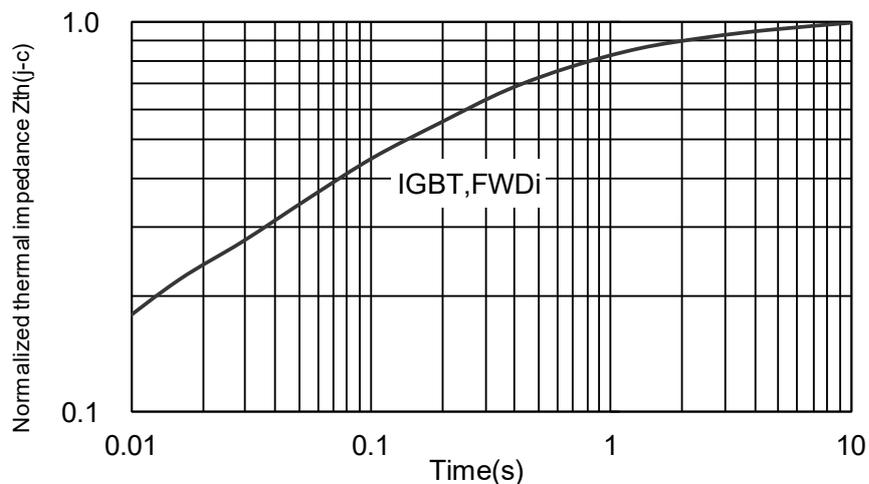


Fig.2-1-4 Typical transient thermal impedance (PSSxxS51F6)

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2.1.3 Electric Characteristics and Recommended Conditions

Table 2-1-3 shows the typical static characteristics and switching characteristics of PSS20S71F6.

Table 2-1-3 Static characteristics and switching characteristics of PSS20S71F6

INVERTER PART ($T_j = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D=V_{DB} = 15\text{V}, V_{IN}= 5\text{V}, I_C= 20\text{A}$	-	1.40	1.90	V	
		$T_j= 25^\circ\text{C}$					
V_{EC}	FWDi forward voltage	$V_{IN}= 0\text{V}, -I_C= 20\text{A}$	-	1.50	2.00	V	
t_{on}	Switching times	$V_{CC}= 300\text{V}, V_D= V_{DB}= 15\text{V}$ $I_C= 20\text{A}, T_j= 125^\circ\text{C}, V_{IN}= 0\leftrightarrow 5\text{V}$ Inductive Load (upper-lower arm)	0.95	1.55	2.15	μs	
$t_{C(on)}$			-	0.50	0.80	μs	
t_{off}			-	1.75	2.35	μs	
$t_{C(off)}$			-	0.40	0.60	μs	
t_{rr}			-	0.30	-	μs	
I_{CES}	Collector-emitter cut-off current	$V_{CE}=V_{CES}$	$T_j= 25^\circ\text{C}$	-	-	1	mA
			$T_j= 125^\circ\text{C}$	-	-	10	

Switching time definition and performance test method are shown in Fig.2-1-4 and 2-1-5. Switching characteristics are measured by half bridge circuit with inductance load.

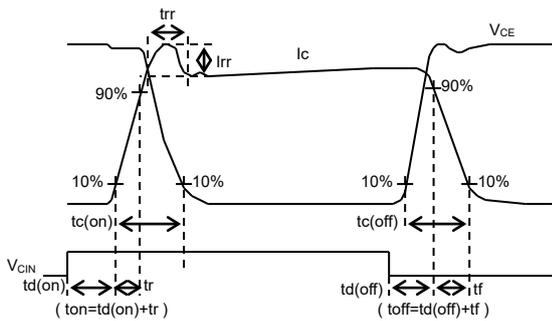


Fig.2-1-5 Switching time definition

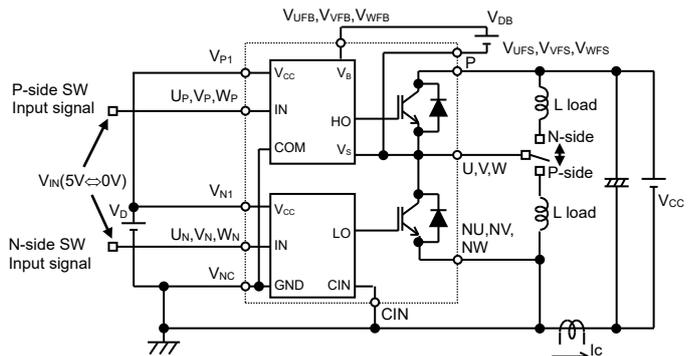


Fig.2-1-6 Evaluation circuit (inductive load)
Short A for N-side IGBT, and short B for P-side IGBT evaluation

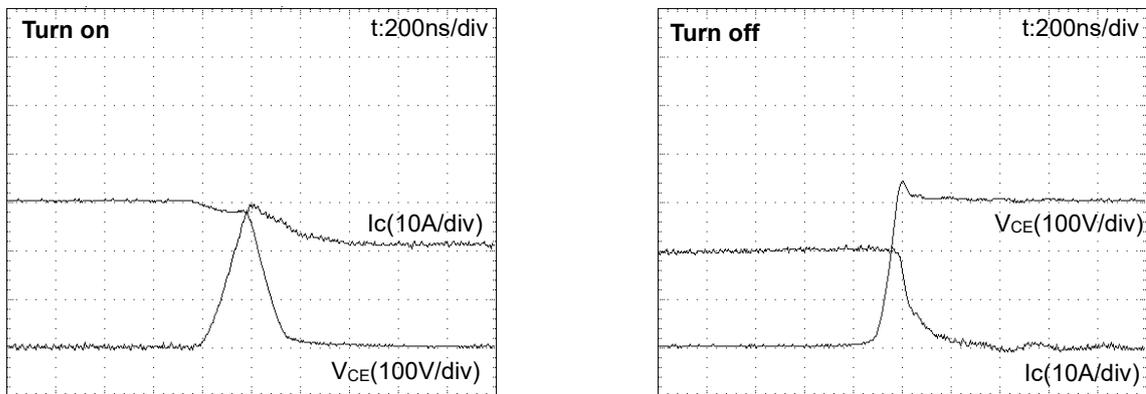


Fig.2-1-7 Typical switching waveform (PSS20S71F6)
Conditions: $V_{CC}=300\text{V}, V_D=V_{DB}=15\text{V}, T_j=125^\circ\text{C}, I_C=20\text{A}$, Inductive load half-bridge circuit

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Table 2-1-4 shows the typical control part characteristics of PSS20S71F6.

Table 2-1-4 Control (Protection) characteristics of PSS20S71F6

CONTROL (PROTECTION) PART ($T_j = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I_D	Circuit current	Total of $V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$	$V_D=15\text{V}$, $V_{IN}=0\text{V}$	-	-	6.00	mA
			$V_D=15\text{V}$, $V_{IN}=5\text{V}$	-	-	6.00	
I_{DB}		Each part of $V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	$V_D=V_{DB}=15\text{V}$, $V_{IN}=0\text{V}$	-	-	0.55	
			$V_D=V_{DB}=15\text{V}$, $V_{IN}=5\text{V}$	-	-	0.55	
$V_{SC(ref)}$	Short circuit trip level	$V_D = 15\text{V}$ (Note 1)	0.45	0.48	0.51	V	
UV_{DBt}	P-side Control supply under-voltage protection(UV)	$T_j \leq 125^\circ\text{C}$	Trip level	10.0	-	12.0	V
UV_{DBr}			Reset level	10.5	-	12.5	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature output	Pull down $R=5\text{k}\Omega$ (Note 2) LVIC Temperature= 85°C	2.51	2.64	2.76	V	
V_{FOH}	Fault output voltage	$V_{SC} = 0\text{V}$, F_O terminal pulled up to 5V by 10k Ω	4.9	-	-	V	
V_{FOL}		$V_{SC} = 1\text{V}$, $I_{FO} = 1\text{mA}$	-	-	0.95	V	
t_{FO}	Fault output pulse width	$C_{FO}=22\text{nF}$ (Note 3)	1.6	2.4	-	ms	
I_{IN}	Input current	$V_{IN} = 5\text{V}$	0.70	1.00	1.50	mA	
$V_{th(on)}$	ON threshold voltage	Applied between U_P , V_P , W_P , U_N , V_N , W_N-V_{NC}	-	2.10	2.60	V	
$V_{th(off)}$	OFF threshold voltage		0.80	1.30	-		
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage		0.35	0.80	-		
V_F	Bootstrap Di forward voltage	$I_F=10\text{mA}$ including voltage drop by limiting resistor	0.5	0.9	1.3	V	
R	Built-in limiting resistance	Included in bootstrap Di	16	20	24	Ω	

- Note 1 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 2 times of the current rating.
 2 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM.
 3 : Fault signal F_O outputs when SC or UV protection works. F_O pulse width is different for each protection modes. At SC failure, F_O pulse width is a fixed width which is specified by the capacitor connected to C_{FO} terminal. ($C_{FO}=9.1 \times 10^{-6} \times t_{FO} [F]$), but at UV failure, F_O outputs continuously until recovering from UV state. (But minimum F_O pulse width is the specified time by C_{FO} .)

Recommended operating conditions of PSS20S71F6 are given in Table 2-1-5. It is highly recommended to operate the modules within these conditions so as to ensure DIPIPM safe operation.

Table 2-1-5 Recommended operating conditions of PSS20S71F6

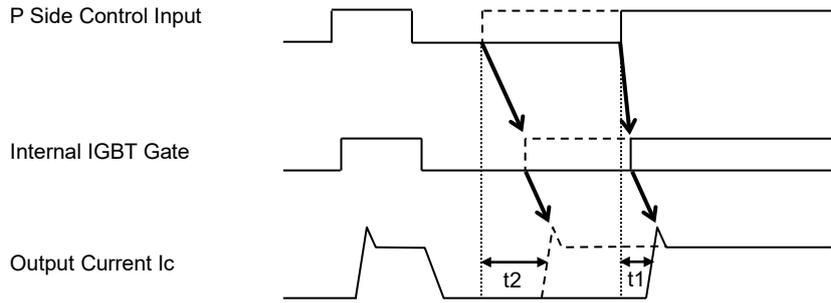
RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V	
V_D	Control supply voltage	Applied between $V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$	13.5	15.0	16.5	V	
V_{DB}	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	13.0	15.0	18.5	V	
$\Delta V_D, \Delta V_{DB}$	Control supply variation		-1	-	+1	V/ μs	
t_{dead}	Arm shoot-through blocking time	For each input signal	1.5	-	-	μs	
f_{PWM}	PWM input frequency	$T_C \leq 100^\circ\text{C}$, $T_j \leq 125^\circ\text{C}$	-	-	20	kHz	
I_O	Allowable r.m.s. current	$V_{CC} = 300\text{V}$, $V_D = 15\text{V}$, P.F = 0.8, Sinusoidal PWM $T_C \leq 100^\circ\text{C}$, $T_j \leq 125^\circ\text{C}$ (Note1)	$f_{PWM} = 5\text{kHz}$	-	-	14.0	Arms
			$f_{PWM} = 15\text{kHz}$	-	-	13.0	
PWIN(on)	Minimum input pulse width	200V $\leq V_{CC} \leq 350\text{V}$, 13.5V $\leq V_D \leq 16.5\text{V}$, 13.0V $\leq V_{DB} \leq 18.5\text{V}$, -20 $^\circ\text{C} \leq T_C \leq 100^\circ\text{C}$, N-line wiring inductance less than 10nH (Note 3)	(Note 2)			-	μs
Below rated current			1.4	-	-		
Between rated current and 1.7 times of rated current			2.5	-	-		
PWIN(off)			Between 1.7 times and 2.0 times of rated current	3.0	-	-	
V_{NC}	V_{NC} variation	Between $V_{NC}-NU$, NV, NW (including surge)	-5.0	-	+5.0	V	
T_j	Junction temperature		-20	-	+125	$^\circ\text{C}$	

- Note 1: Allowable r.m.s. current depends on the actual application conditions.
 2: DIPIPM might not make response if the input signal pulse width is less than PWIN(on)
 3: IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off). Please refer below about delayed response.

Mini DIIPM with BSD Series APPLICATION NOTE

Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P-side only)



Real line: off pulse width > PWIN(off); turn on time t1
 Broken line: off pulse width < PWIN(off); turn on time t2
 (t1:Normal switching time)

About Control supply variation

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

$$dV/dt \leq \pm 1V/\mu s, \quad V_{ripple} \leq 2V_{p-p}$$

2.1.4 Mechanical Characteristics and Ratings

The mechanical characteristics and ratings are shown in Table 2-1-6.
 Please refer to Section 2.4 for the detailed mounting instruction of Mini DIIPM.

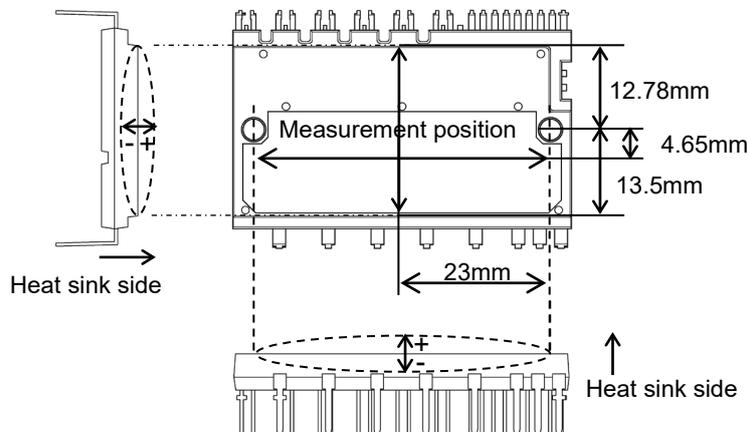
Table 2-1-6 Mechanical characteristics and ratings of PSS20S71F6

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 1)	Recommended 0.78 N·m	0.59	-	0.98	N·m
Terminal pulling strength	Load 9.8N	JEITA-ED-4701	10	-	-	s
Terminal bending strength	Load 4.9N 90deg. bend	JEITA-ED-4701	2	-	-	times
Weight			-	21	-	g
Heat radiation part flatness		(Note 2)	-50	-	100	μm

Note 1: Plain washers (ISO 7089~7094) are recommended.

Note 2: Measurement positions of heat radiation part flatness are as below.



Mini DIIPM with BSD Series APPLICATION NOTE

2.2 Protective Functions and Operating Sequence

Mini DIIPM has Short circuit (SC), Under Voltage of control supply (UV) and temperature output (VOT) for protection function. The operating principle and sequence are described below.

2.2.1 Short Circuit Protection

1. General

Mini DIIPM uses external shunt resistor for the current detection as shown in Fig.2-2-1. The internal protection circuit inside the IC captures the excessive large current by comparing the CIN voltage generated at the shunt resistor with the referenced SC trip voltage, and perform protection automatically. The threshold voltage trip level of the SC protection $V_{sc(ref)}$ is typ. 0.48V.

In case of SC protection happens, all the gates of N-side three phase IGBTs will be interrupted together with a fault signal output. To prevent DIIPM erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter (time constant: $1.5\mu \sim 2\mu s$) to the CIN terminal input (Fig.2-2-1, 2-2-2). Also, please make the pattern wiring around the shunt resistor as short as possible.

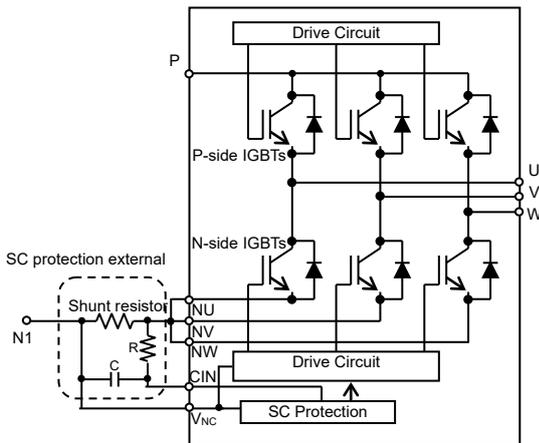


Fig.2-2-1 SC protecting circuit

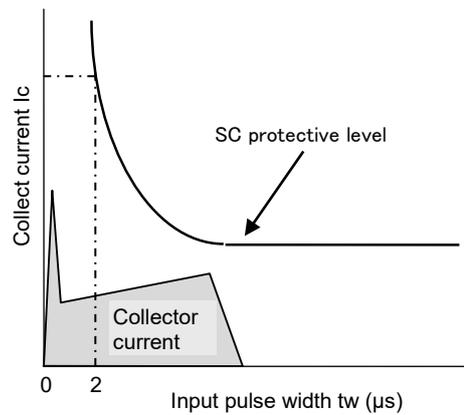


Fig.2-2-2 Filter time constant setting

2. SC protection Sequence

SC protection (N-side only with the external shunt resistor and RC filter)

- a1. Normal operation: IGBT ON and carrying current.
- a2. Short circuit current detection (SC trigger).
It is necessary to set RC time constant so that IGBT shut down within $2.0\mu s$ when SC. ($1.5\sim 2.0\mu s$ is recommended generally.)
- a3. All N-side IGBTs' gate are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. Fo outputs. The pulse width of the Fo signal is set by the external capacitor C_{FO} .
- a6. Input = "L". IGBT OFF
- a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
IGBT of each phase can return to normal state by inputting ON signal to each phase.
- a8. Normal operation: IGBT ON and outputs current.

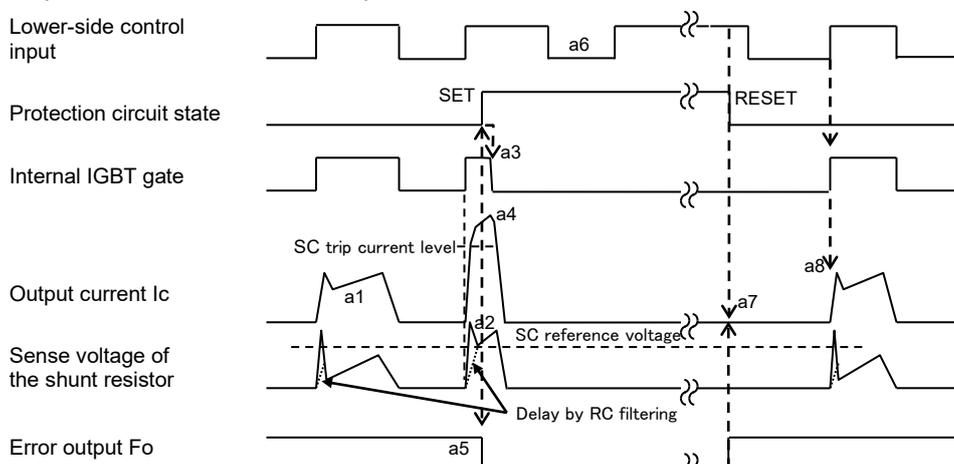


Fig.2-2-3 SC protection timing chart

Mini DIIPM with BSD Series APPLICATION NOTE

3. Determination of Shunt Resistance

(1) Shunt resistance

The value of current sensing resistance is calculated by the following formula:

$$R_{Shunt} = V_{SC(ref)} / SC$$

where $V_{SC(ref)}$ is the SC trip voltage.

The maximum SC trip level $SC(max)$ should be set less than the IGBT minimum saturation current which is 2.0 times as large as the rated current. For example, the $SC(max)$ of PSS20S71F6 should be set to $20 \times 2 = 40A$. The parameters ($V_{SC(ref)}$, R_{Shunt}) dispersion should be considered when designing the SC trip level.

For example of PSS20S71F6, there is $\pm 0.03V$ dispersion in the spec of $V_{SC(ref)}$ as shown in Table 2-2-1.

Table 2-2-1 Specification for $V_{SC(ref)}$ (unit: V)

Condition	Min	Typ	Max
at $T_j = 25^\circ C$, $V_D = 15V$	0.45	0.48	0.51

Then, the range of SC trip level can be calculated by the following expressions:

$$R_{Shunt(min)} = V_{SC(ref) max} / SC(max)$$

$$R_{Shunt(typ)} = R_{Shunt(min)} / 0.95^* \quad \text{then} \quad SC(typ) = V_{SC(ref) typ} / R_{Shunt(typ)}$$

$$R_{Shunt(max)} = R_{Shunt(typ)} \times 1.05^* \quad \text{then} \quad SC(min) = V_{SC(ref) min} / R_{Shunt(max)}$$

**) This is the case that shunt resistance dispersion is within $\pm 5\%$.*

So the SC trip level range is described as Table 2-2-2.

Table 2-2-2 Operative SC Range ($R_{Shunt} = 12.8m\Omega$ (min), $13.4m\Omega$ (typ), $14.1m\Omega$ (max))

Condition	min.	typ.	Max.
at $T_j = 25^\circ C$, $V_D = 15V$	31.9A	35.8A	40A

(e.g. $12.8m\Omega$ ($R_{Shunt(min)} = 0.51V (=V_{SC(max)}) / 40A (=SC(max))$)

There is the possibility that the actual SC protection level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. It is recommended to make a confirmation of the resistance by prototype experiment.

(2) RC Filter Time Constant

It is necessary to set an RC filter in the SC sensing circuit in order to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCOA of the DIIPM.

When the voltage drop on the external shunt resistor exceeds the SC trip level, The time (t_1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - e^{-\frac{t_1}{\tau}})$$

$$t_1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

V_{sc} : the CIN terminal input voltage, I_c : the peak current, τ : the RC time constant

On the other hand, the typical time delay t_2 (from V_{sc} voltage reaches $V_{sc(ref)}$ to IGBT gate shutdown) of IC is shown in Table 2-2-3.

Table 2-2-3 Internal time delay of IC

Item	Min	typ	max	Unit
IC transfer delay time	-	-	1.0	μs

Therefore, the total delay time from an SC level current happened to the IGBT gate shutdown becomes:

$$t_{TOTAL} = t_1 + t_2$$

Mini DIIPM with BSD Series APPLICATION NOTE

2.2.2 Control Supply UV Protection

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-2-4.

Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10 μ s) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10 μ s after UV happened.

Table 2-2-4 DIIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	In this voltage range, built-in control IC may not work properly. Normal operating of each protection function (UV, Fo output etc.) is not also assured. Normally IGBT does not work. But external noise may cause DIIPM malfunction (turns ON), so DC-link voltage need to start up after control supply starts-up.
4.0-UV _{Dt} (N), UV _{DBt} (P)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
UV _{Dt} (N)-13.5V UV _{DBt} (P)-13.0V	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N) 13.0-18.5V (P)	Recommended conditions.
16.5-20.0V (N) 18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	The control circuit might be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$$dV/dt \leq \pm 1V/\mu s, \quad V_{\text{ripple}} \leq 2V_{\text{p-p}}$$

Mini DIIPM with BSD Series APPLICATION NOTE

[N-side UV Protection Sequence]

- a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal ($L \rightarrow H$). (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a2. Normal operation: IGBT ON and carrying current.
- a3. V_D level dips to under voltage trip level. (UV_{Dt}).
- a4. All N-side IGBTs turn OFF in spite of control input condition.
- a5. F_o outputs for the period set by the capacitance C_{FO} , but output is extended during V_D keeps below UV_{Dr} .
- a6. V_D level reaches UV_{Dr} .
- a7. Normal operation: IGBT ON and outputs current.

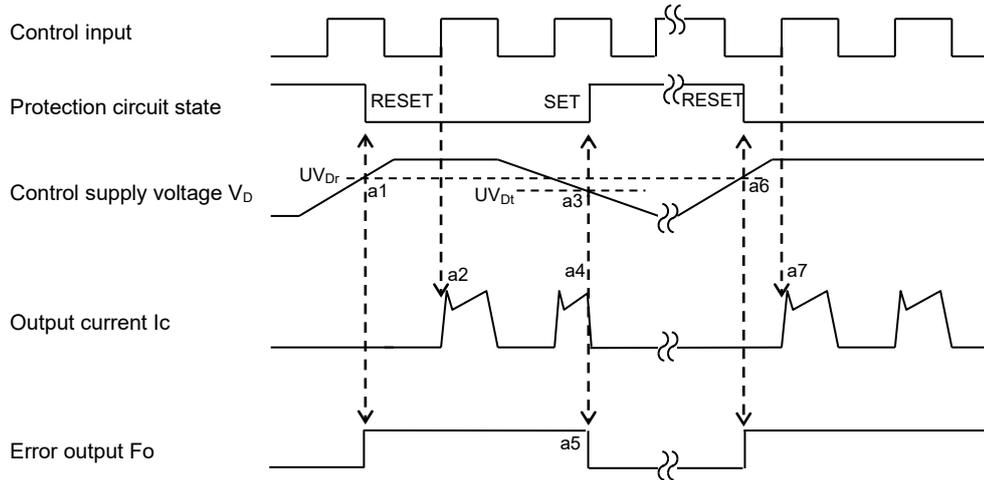


Fig.2-2-4 Timing chart of N-side UV protection

[P-side UV Protection Sequence]

- a1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr} , IGBT turns on by next ON signal ($L \rightarrow H$).
- a2. Normal operation: IGBT ON and outputs current.
- a3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
- a4. IGBT of the corresponding phase only turns OFF in spite of control input signal level, but there is no F_o signal output.
- a5. V_{DB} level reaches UV_{DBr} .
- a6. Normal operation: IGBT ON and outputs current.

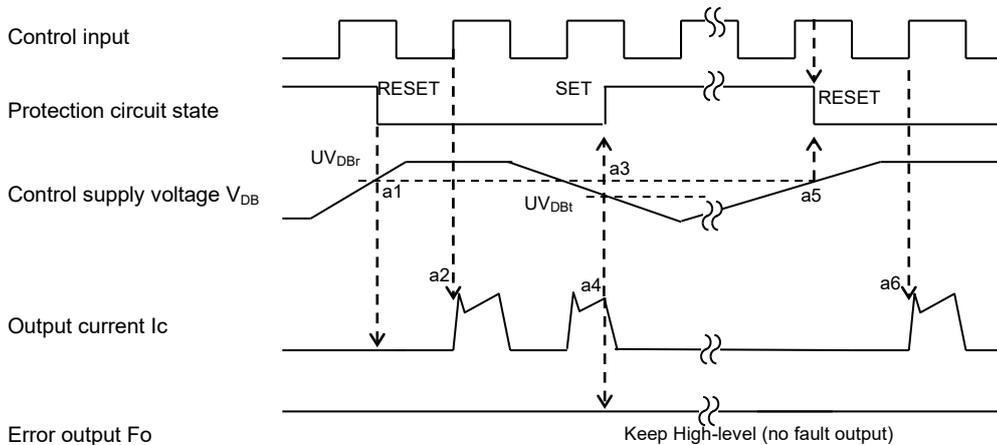


Fig.2-2-5 Timing Chart of P-side UV protection

Mini DIIPM with BSD Series APPLICATION NOTE

2.2.3 Temperature output function V_{OT}

(1) Usage of this function

This function measures the temperature of control LVIC by built in temperature sensor on LVIC.

The heat generated at IGBT and FWDi transfers to LVIC through molding resin of package and outer heat sink. So LVIC temperature cannot respond to rapid temperature rise of those power chips effectively. (e.g. motor lock, short circuit) It is recommended to use this function for protecting from slow excessive temperature rise by such cooling system down and continuance of overload operation. (Replacement from the thermistor which was mounted on outer heat sink currently)

[Note]

In this function, DIIPM cannot shutdown IGBT and output fault signal by itself when temperature rises excessively. When temperature exceeds the defined protection level, controller (MCU) should stop the DIIPM.

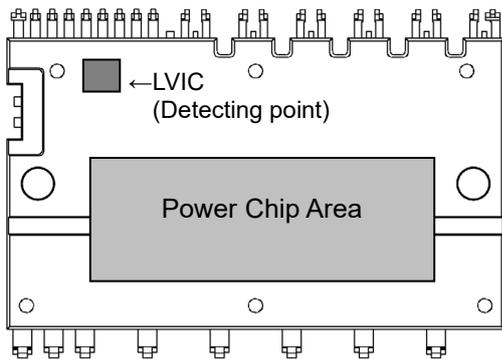


Fig.2-2-6 Temperature detecting point

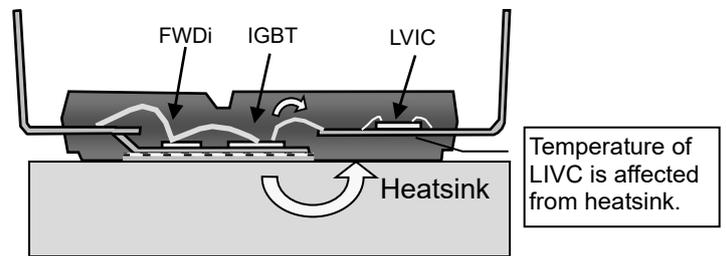


Fig.2-2-7 Thermal conducting from power chips

(2) V_{OT} characteristics

V_{OT} output circuit, which is described in Fig.2-2-9, is the output of OP amplifier circuit. The current capability of V_{OT} output is described as Table 2-2-6. The characteristics of V_{OT} output vs. LVIC temperature are linear characteristics described in Fig 2-2-12 and Fig.2-2-13. There are some cautions for using this function as below.

Table 2-2-6 Output capability
($T_c = -20^\circ\text{C} \sim 100^\circ\text{C}$)

	min.
Source	1.7mA
Sink	0.1mA

Source: Current flow from V_{OT} to outside.

Sink : Current flow from outside to V_{OT} .

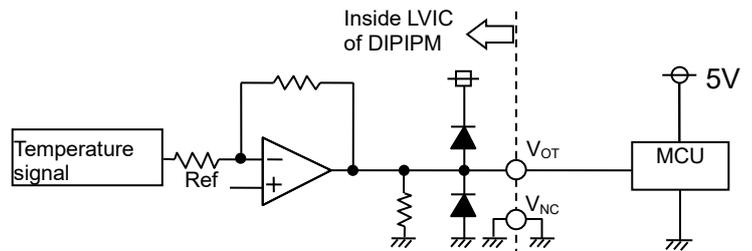


Fig.2-2-8 V_{OT} output circuit

• In the case of detecting lower temperature than room temperature

It is recommended to insert 5.1k Ω pull down resistor for getting linear output characteristics at lower temperature than room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra current calculated by V_{OT} output voltage / pull down resistance flows as LVIC circuit current continuously. In the case of only using V_{OT} for detecting higher temperature than room temperature, it isn't necessary to insert the pull down resistor.

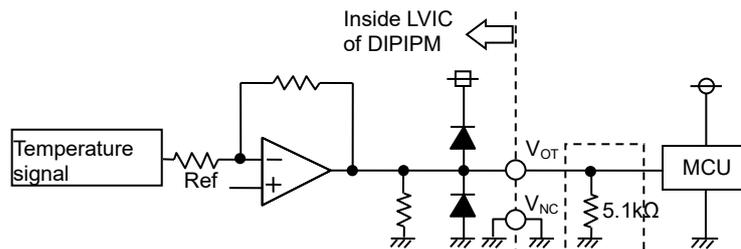


Fig.2-2-9 V_{OT} output circuit in the case of detecting low temperature

Mini DIIPM with BSD Series APPLICATION NOTE

• In the case of using with low voltage controller(MCU)

In the case of using V_{OT} with low voltage controller (e.g. 3.3V MCU), V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and this output for preventing over voltage.

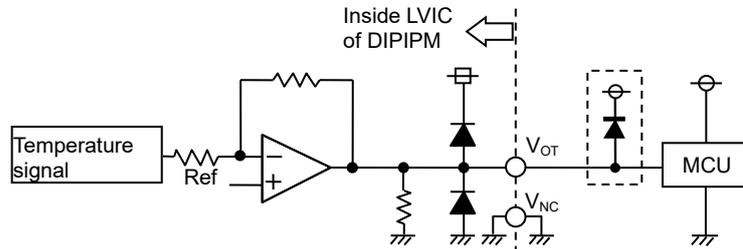


Fig.2-2-10 V_{OT} output circuit in the case of using with low voltage controller

• In the case that the protection level exceeds control supply of the controller

In the case of using low voltage controller like 3.3V MCU, if it is necessary to set the trip V_{OT} level to control supply voltage (e.g. 3.3V) or more, there is the method of dividing the V_{OT} output by resistance voltage divider circuit and then inputting to A/D converter on MCU (Fig.2-2-11). In that case, sum of the resistances of divider circuit should be almost 5.1k Ω . About the necessity of clamp diode, we consider that the divided output will not exceed the supply voltage of controller generally, so it will be unnecessary to insert the clamp diode. But it should be judged by the divided output level finally.

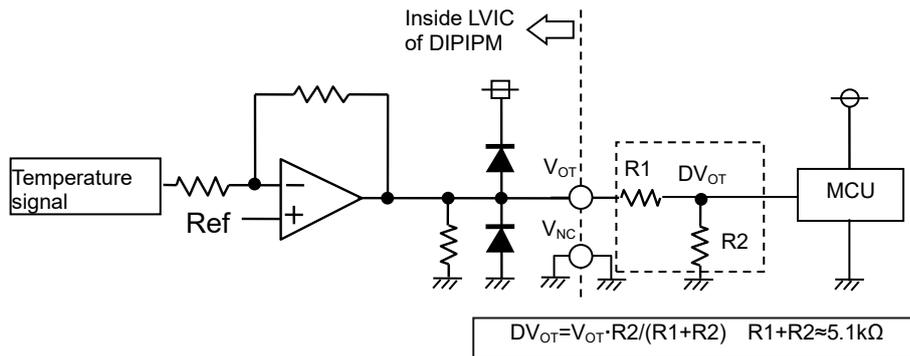


Fig.2-2-11 V_{OT} output circuit in the case with high protection level

Mini DIIPM with BSD Series APPLICATION NOTE

Please handle the following characteristics of VOT output vs. LVIC temperature as reference data to set over temperature protection. These curves are based on theoretical designed value excluding specified value in the target specification.

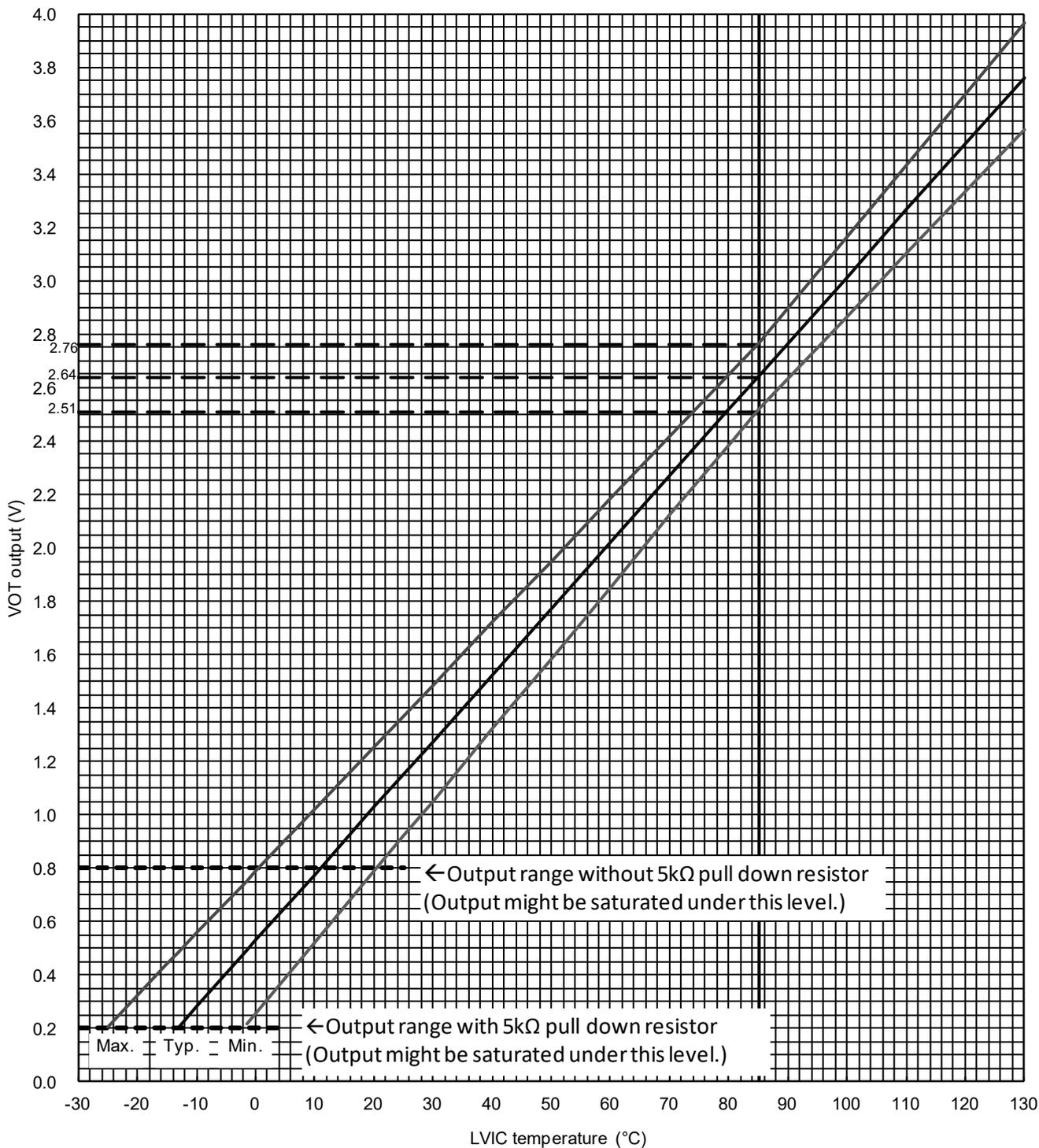


Fig.2-2-12 V_{OT} output vs. LVIC temperature (PSSxxS71F6)

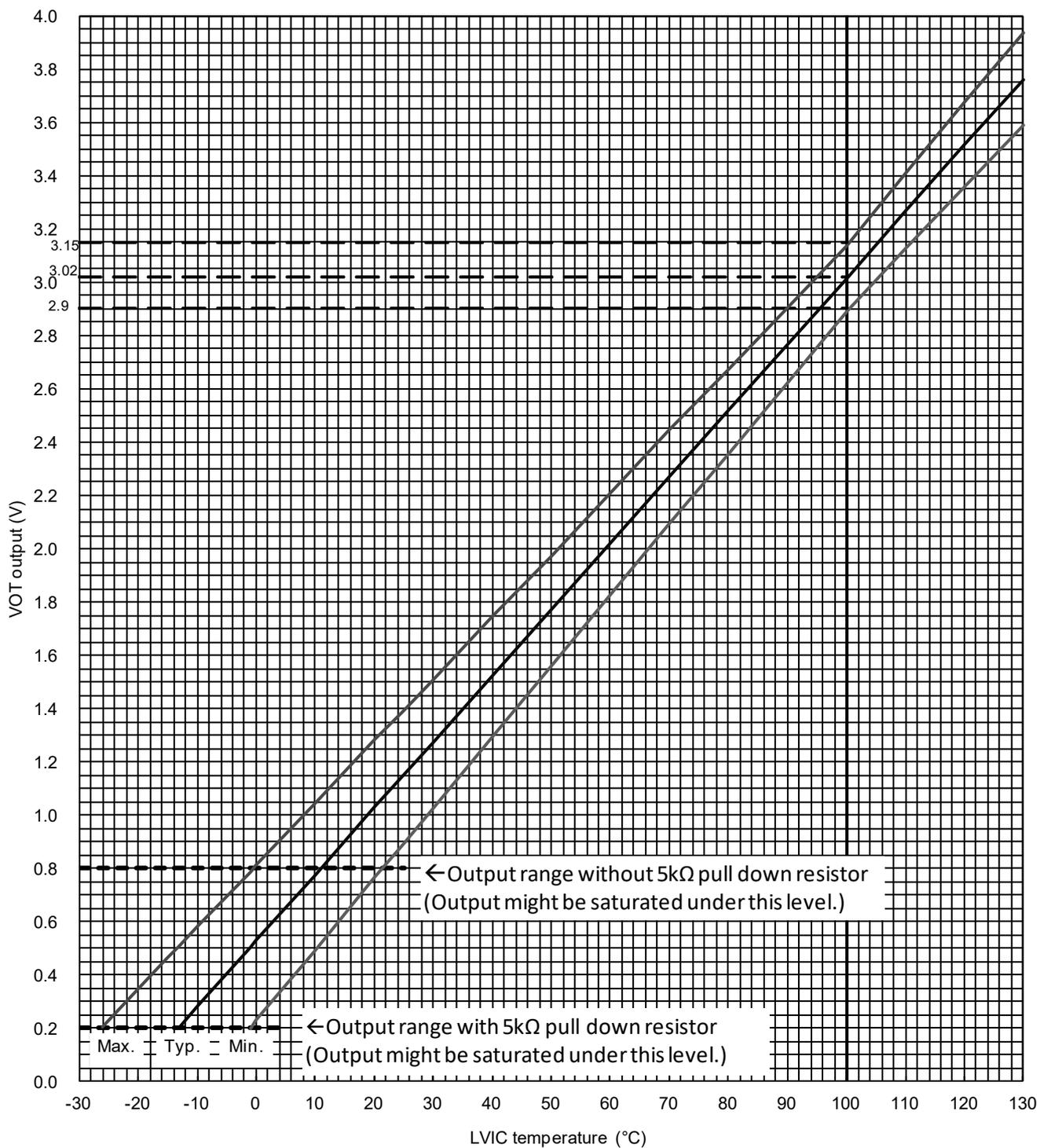


Fig.2-2-13 V_{OT} output vs. LVIC temperature (PSSxxS51F6)

Mini DIIPM with BSD Series APPLICATION NOTE

(3) Usage of V_{OT} function

As mentioned above, the heat of power chips transfers to LVIC through the heat sink and package, so the relationship between LVIC temperature: $T_{ic}(=V_{OT}$ output), case temperature: T_c (under the chip defined on datasheet), and junction temperature: T_j depends on the system cooling condition, heat sink, control strategy, etc. For example of PSSxxS71F6, their relationship example in the case of using the heat sink (Table 2-2-7) is described in Fig.2-2-14. This relationship may be different due to the cooling conditions. So when setting the threshold temperature for protection, it is necessary to get the relationship between them on your real system. And when setting threshold temperature T_{ic} , it is important to consider the protection temperature keeps $T_j \leq 150^\circ\text{C}$.

Table 2-2-7 Outer heat sink

Heat sink size (W x D x H)
200 x 85 x 40 mm

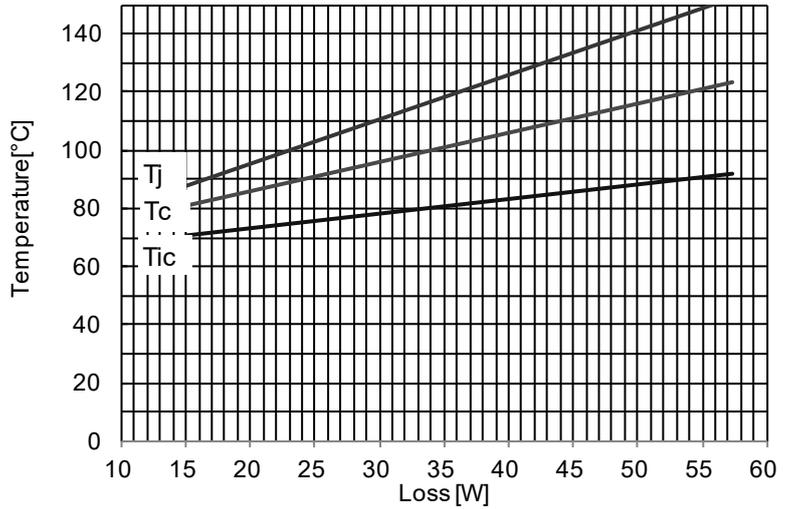
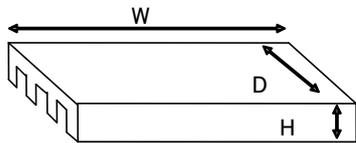


Fig.2-2-14 Example of relationship of T_j , T_c , T_{ic}
(One IGBT chip turns on. DC current $T_a=25^\circ\text{C}$)

Procedure about setting the protection level by using Fig.2-2-15 is described as below.

Table 2-2-8 Procedure for setting protection level

	Procedure	Setting value example
1)	Set the protection T_j temperature	Set T_j to 135°C as protection level.
2)	Get LVIC temperature T_{ic} that matches to above T_j of the protection level from the relationship of T_j - T_{ic} in Fig.2-2-15.	$T_{ic}=85^\circ\text{C}$ (@ $T_j=135^\circ\text{C}$)
3)	Get V_{OT} value from the V_{OT} output characteristics in Fig.2-2-16 and the T_{ic} value which was obtained at phase 2).	$V_{OT}=2.64\text{V}$ (@ $T_{ic}=85^\circ\text{C}$) is decided as the protection level.

As above procedure, the setting value for V_{OT} output is decided to 2.64V. But V_{OT} output has some data spread, so it is important to confirm whether the protection temperature fluctuation of T_j is not $T_j > 150^\circ\text{C}$ due to the data spread of V_{OT} output. Procedure about the confirmation of temperature fluctuation is described in Table 2-2-9.

Table 2-2-9 Procedure for confirmation of temperature fluctuation

	Procedure	Confirmation example
4)	Confirm the region of T_{ic} fluctuation at above V_{OT} from Fig.2-2-16.	$T_{ic}=80^\circ\text{C}\sim 90^\circ\text{C}$ (@ $V_{OT}=2.64\text{V}$)
5)	Confirm the region of T_j fluctuation at above region of T_{ic} from Fig.2-2-15.	$T_j=117^\circ\text{C}\sim 147^\circ\text{C}$ ($\leq 150^\circ\text{C}$ No problem) In this case, fluctuation of T_c is $T_c=100^\circ\text{C}\sim 120^\circ\text{C}$

Mini DIIPM with BSD Series APPLICATION NOTE

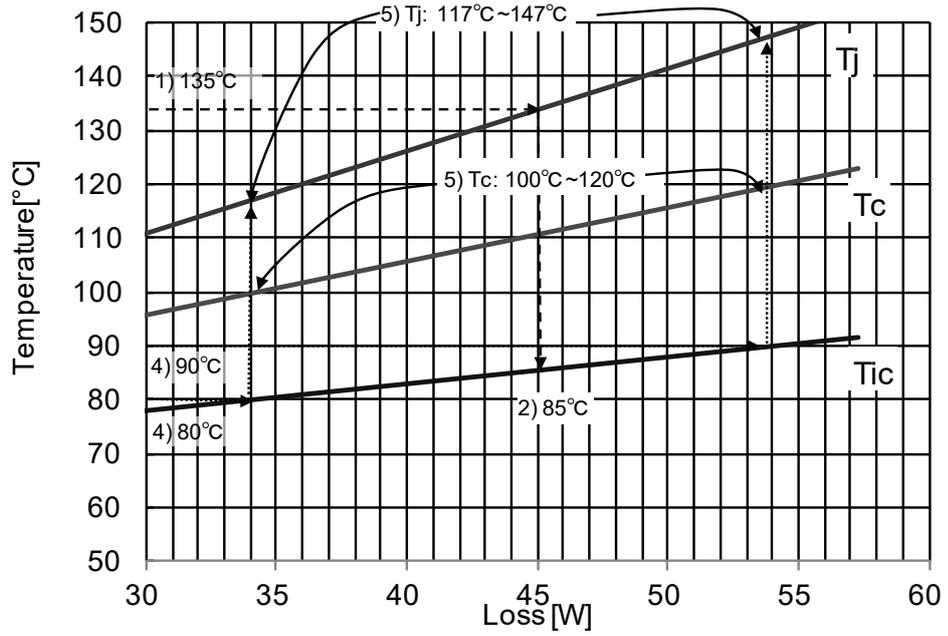


Fig.2-2-15 Relationship of T_j , T_c , T_{ic} (Enlarged graph of Fig.2-2-14)

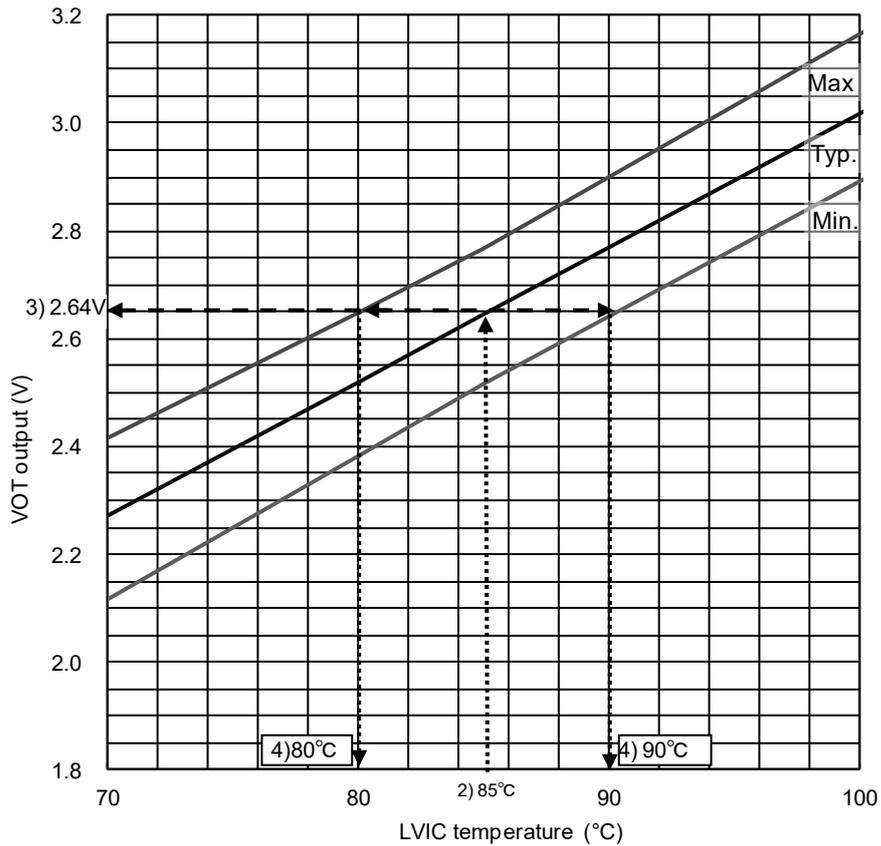


Fig.2-2-16 V_{OT} output vs. LVIC temperature (Enlarged graph of Fig.2-2-12)

The relationship between T_{ic} , T_c (measuring) and T_j (calculated by loss) depends on the system cooling condition and control strategy, and so on. So please evaluate about these temperature relationship on your real system when considering the protection level.

If necessary, it is possible to ship the sample with the individual data of V_{OT} vs. LVIC temperature.

Mini DIIPM with BSD Series APPLICATION NOTE

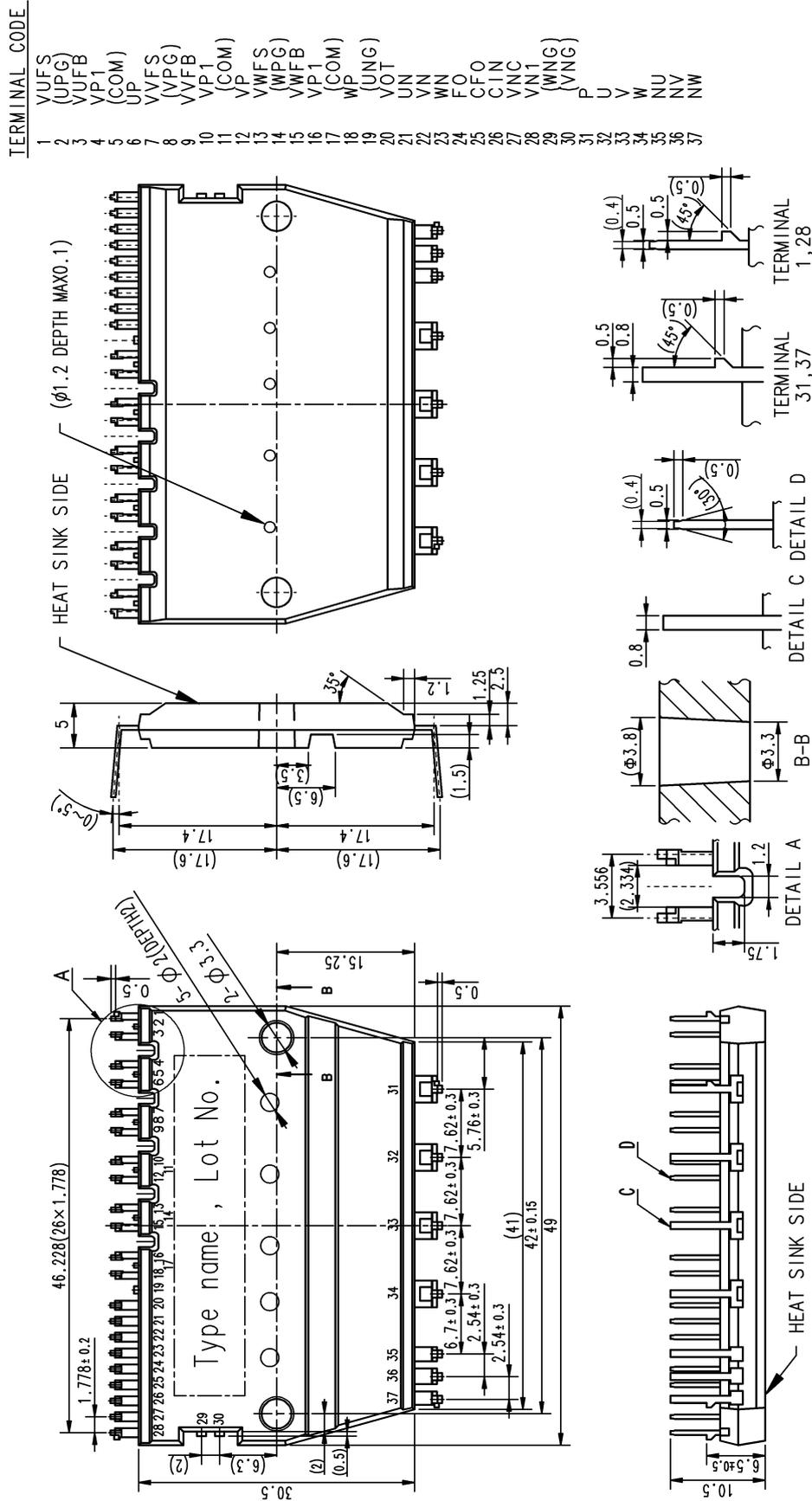


Fig.2-3-2 PSSxxS51F6 short terminal type package outline drawing (Dimension in mm)

Mini DIIPM with BSD Series APPLICATION NOTE

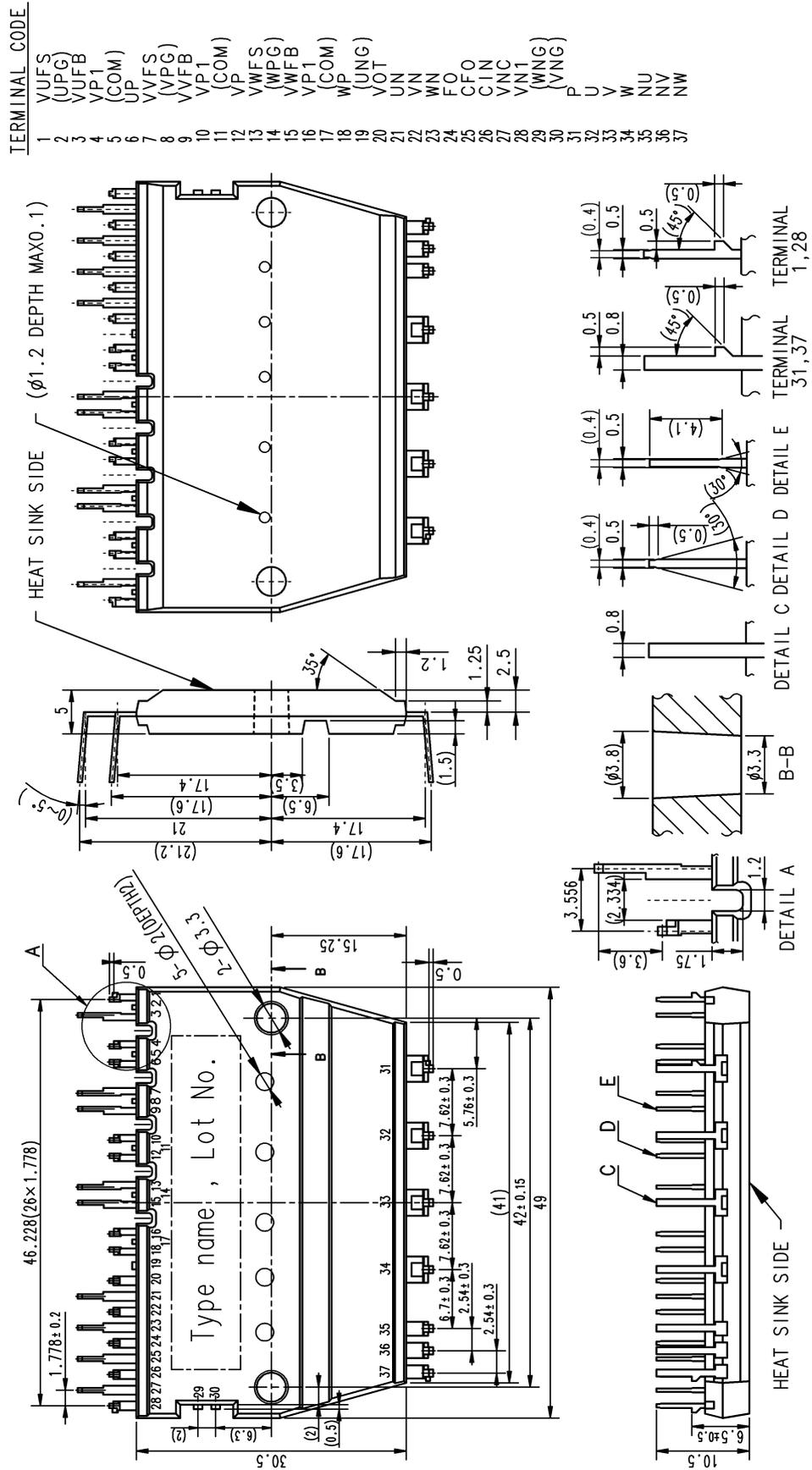


Fig.2-3-3 PSSxxS51F6-C control side zigzag terminal type package outline drawing (Dimension in mm)

Mini DIIPM with BSD Series APPLICATION NOTE

2.3.3 Terminal Description

Table 2-3-1 Terminal description (PSSxxS71F6)

No.	Symbol	Description
1	V _{UFS}	U-phase P-side drive supply GND terminal
2	(UPG)	Dummy-pin
3	V _{UFB}	U-phase P-side drive supply positive terminal
4	V _{P1}	U-phase P-side control supply positive terminal
5	(COM)	Dummy-pin
6	U _P	U-phase P-side control input terminal
7	V _{VFS}	V-phase P-side drive supply GND terminal
8	(VPG)	Dummy-pin
9	V _{VFB}	V-phase P-side drive supply positive terminal
10	V _{P1}	V-phase P-side control supply positive terminal
11	(COM)	Dummy-pin
12	V _P	V-phase P-side control input terminal
13	V _{WFS}	W-phase P-side drive supply GND terminal
14	(WPG)	Dummy-pin
15	V _{WFB}	W-phase P-side drive supply positive terminal
16	V _{P1}	W-phase P-side control supply positive terminal
17	COM	Dummy-pin
18	W _P	W-phase P-side control input terminal
19	(UNG)	Dummy-pin
20	V _{OT}	Temperature output ^{*2)}
21	U _N	U-phase N-side control input terminal
22	V _N	V-phase N-side control input terminal
23	W _N	W-phase N-side control input terminal
24	F _O	Fault signal output terminal
25	CFO	Fault pulse output width setting terminal
26	CIN	SC current trip voltage detecting terminal
27	V _{NC}	N-side control supply GND terminal
28	V _{N1}	N-side control supply positive terminal
29	(WNG)	Dummy-pin
30	(VNG)	Dummy-pin
31	NW	WN-phase IGBT emitter
32	NV	VN-phase IGBT emitter
33	NU	UN-phase IGBT emitter
34	W	W-phase output terminal
35	V	V-phase output terminal
36	U	U-phase output terminal
37	P	Inverter DC-link positive terminal
38	NC	No connection

Table 2-3-2 Terminal description (PSSxxS51F6)

No.	Symbol	Description
1	V _{UFS}	U-phase P-side drive supply GND terminal
2	(UPG)	Dummy-pin
3	V _{UFB}	U-phase P-side drive supply positive
4	V _{P1}	U-phase P-side control supply positive
5	(COM)	Dummy-pin
6	U _P	U-phase P-side control input terminal
7	V _{VFS}	V-phase P-side drive supply GND terminal
8	(VPG)	Dummy-pin
9	V _{VFB}	V-phase P-side drive supply positive terminal
10	V _{P1}	V-phase P-side control supply positive terminal
11	(COM)	Dummy-pin
12	V _P	V-phase P-side control input terminal
13	V _{WFS}	W-phase P-side drive supply GND terminal
14	(WPG)	Dummy-pin
15	V _{WFB}	W-phase P-side drive supply positive terminal
16	V _{P1}	W-phase P-side control supply positive terminal
17	(COM)	Dummy-pin
18	W _P	W-phase P-side control input terminal
19	(UNG)	Dummy-pin
20	V _{OT}	Temperature output ^{*2)}
21	U _N	U-phase N-side control input terminal
22	V _N	V-phase N-side control input terminal
23	W _N	W-phase N-side control input terminal
24	F _O	Fault signal output terminal
25	CFO	Fault pulse output width setting terminal
26	CIN	SC current trip voltage detecting terminal
27	V _{NC}	N-side control supply GND terminal
28	V _{N1}	N-side control supply positive terminal
29	(WNG)	Dummy-pin
30	(VNG)	Dummy-pin
31	P	Inverter DC-link positive terminal
32	U	U-phase output terminal
33	V	V-phase output terminal
34	W	W-phase output terminal
35	NU	UN-phase IGBT emitter
36	NV	VN-phase IGBT emitter
37	NW	WN-phase IGBT emitter

- 1) Dummy pin has some potential like gate voltage. Don't connect all dummy-pins to any other terminals or PCB pattern.
- 2) About No.20 terminal, it is assigned the different function from current Mini DIIPM Ver.3 and Ver.4 series. For more detail information, refer following table.

Table 2-3-3 Difference between this series and former products

Part Number	Mini DIP Ver.3			Mini DIP Ver.4	This series
		PS21562 PS21563	PS2156x-SP	PS21564 PS21565	PS21765 PS21767
Symbol	V _{NO}				V _{OT}
Connected destination	To GND(V _{NC})		NC (no connection)	To GND(V _{NC})	To A/D input of MCU or NC(in the case of not using V _{OT})

Mini DIIPM with BSD Series APPLICATION NOTE

Table 2-3-4 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal	V_{UFB} - V_{UFS} V_{VFB} - V_{VFS} V_{WFB} - V_{WFS}	<ul style="list-style-type: none"> Drive supply terminals for P-side IGBTs. By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIIPM P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply during ON-state of the corresponding N-side IGBT in the loop. Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side drive supply GND terminal		
P-side control supply terminal	V_{P1} V_{N1}	<ul style="list-style-type: none"> Control supply terminals for the built-in HVIC and LVIC. In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with good frequency characteristics should be mounted very closely to these terminals. Design the supply carefully so that the voltage ripple caused by operation keep within the specification. ($dV/dt \leq \pm 1V/\mu s$, $V_{ripple} \leq 2Vp-p$) It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control supply terminal		
N-side control GND terminal	V_{NC}	<ul style="list-style-type: none"> Control ground terminal for the built-in HVIC and LVIC. Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P, V_P, W_P U_N, V_N, W_N	<ul style="list-style-type: none"> Control signal input terminals. Voltage input type. These terminals are internally connected to Schmitt trigger circuit and pulled down by min 2.5kΩ resistor internally The wiring of each input should be as short as possible to protect the DIIPM from noise interference. Use RC coupling in case of signal oscillation. Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor.
Short-circuit trip voltage detecting terminal	CIN	<ul style="list-style-type: none"> For short circuit protection, input the potential of external shunt resistor to CIN terminal through RC filter (for the noise immunity). The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	Fo	<ul style="list-style-type: none"> Fault signal output terminal. Fo signal line should be pulled up to the logic supply. (In the case pulling up to 5V supply, over 5kΩ resistor is needed for limiting the Fo sink current I_{Fo} up to 1mA. Normally 10kΩ is recommended.)
Fault pulse output width setting terminal	CFO	<ul style="list-style-type: none"> The terminal is for setting Fo pulse width by connecting capacitor between V_{NC}. When 22nF is connected, then the Fo pulse width becomes typ. 2.4ms. $C_{FO} (F) = 9.1 \times 10^{-6} \times t_{FO}$ (Required Fo pulse width)
Temperature output terminal	V_{OT}	<ul style="list-style-type: none"> LVIC temperature is output by analog signal. This terminal is connected to the output of OP amplifier internally. It is recommended to connect 5.1kΩ pulldown resistor if output linearity is necessary under room temperature.
Inverter DC-link positive terminal	P	<ul style="list-style-type: none"> DC-link positive power supply terminal. Internally connected to the collectors of all P-side IGBTs. To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU, NV, NW	<ul style="list-style-type: none"> Open emitter terminal of each N-side IGBT These terminals are connected to the power GND through individual shunt resistor.
Inverter power output terminal	U, V, W	<ul style="list-style-type: none"> Inverter output terminals for connection to inverter load (e.g. AC motor). Each terminal is internally connected to the intermediate point of the corresponding IGBT half bridge arm.

Note: 1) Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1 μs /div. Please ensure the voltage (including surge) not exceed the specified limitation.

Mini DIIPM with BSD Series APPLICATION NOTE

2.4 Mounting Method

This section shows the electric spacing and mounting precautions of Mini DIIPM.

2.4.1 Electric Spacing

The electric spacing specification of Mini DIIPM is shown in Table 2-4-1

Table 2-4-1 Minimum insulation distance of PSSxxS71F6 (minimum value)

Clearance(mm)		Creepage(mm)	
Between power terminals	4.0	Between power terminals	4.0
Between control terminals	2.5	Between control terminals	6.0
Between terminals and heat sink	3.0	Between terminals and heat sink	4.0

Table 2-4-2 Minimum insulation distance of PSSxxS51F6 (minimum value)

Clearance(mm)		Creepage(mm)	
Between power terminals	4.0	Between power terminals	4.0
Between control terminals	1.8	Between control terminals	4.0
Between terminals and heat sink	2.3	Between terminals and heat sink	2.3*(4.0)

***) About creepage between dummy terminals and heat sink of PSSxxS51F6**

The creepage between dummy terminal and heat sink (gate potential of VN IGBT and WN IGBT) on the side of DIIPM is min.2.3mm. Also, the creepage (X) between screw or washer and terminal may be 4mm or less due to the washer size.

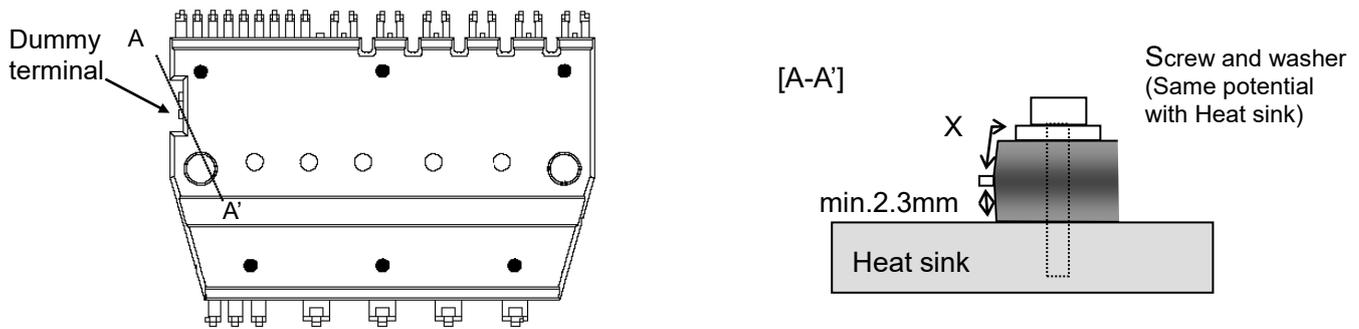
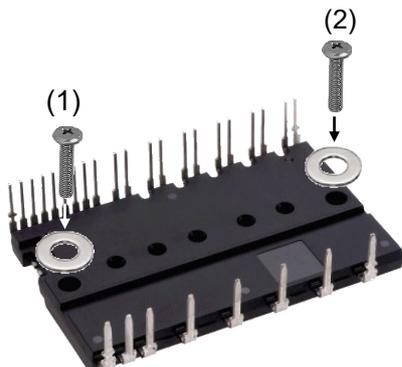


Fig.2-4-1 Creepage between dummy terminal and heat sink

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the chips or insulation structure. The recommended fastening procedure is shown in Fig.2-4-2. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. And pay attention not to have any foreign particle on the contact surface between the module and the heat sink. Even if the fixing of heatsink was done by proper procedure and condition, there is a possibility of damaging the package because of tightening by unexpected excessive torque or tucking particle. For ensuring safety it is recommended to conduct the confirmation test(e.g. insulation inspection) on the final product after fixing the DIIPM with the heatsink.



Temporary fastening
(1)→(2)

Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating. Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-4-2 Recommended screw fastening order

Mini DIIPM with BSD Series APPLICATION NOTE

Table 2-4-2 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Screw : M3	0.59	0.78	0.98	N·m
Flatness of outer heat sink	Refer Fig.2-4-3	-50	-	+100	μm

Note : Recommend to use plain washer (ISO7089-7094) in fastening the screws.

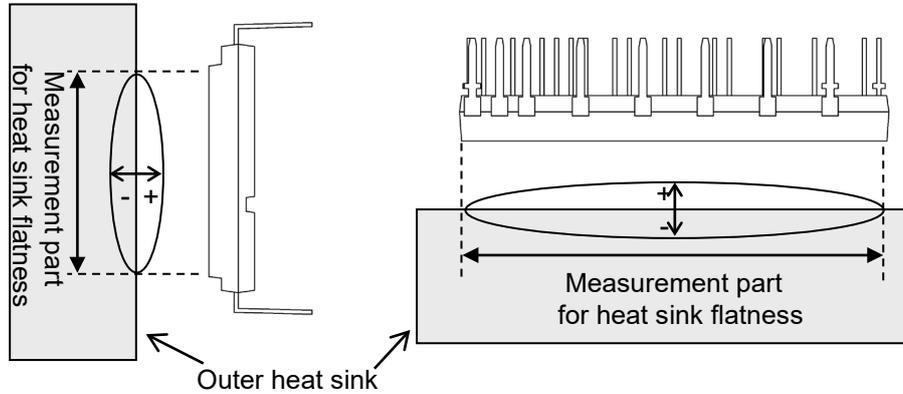


Fig.2-4-3 Measurement point of heat sink flatness (PSSxxS71F6)

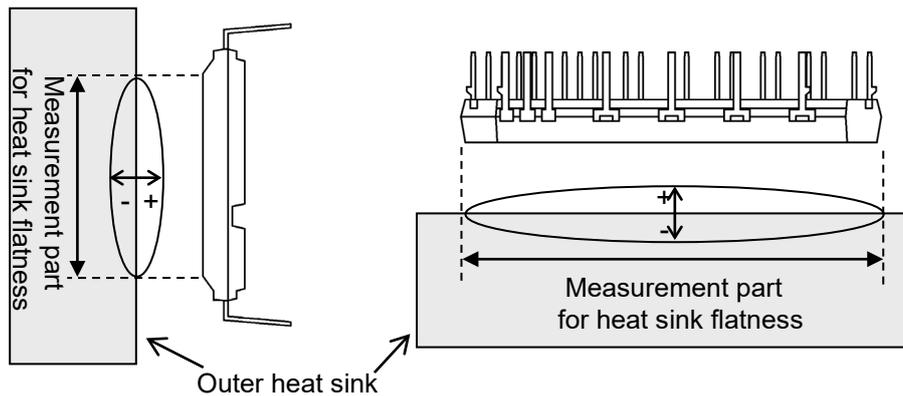


Fig.2-4-4 Measurement point of heat sink flatness (PSSxxS51F6)

In order to get effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp/concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermal conductive grease with 100μ-200μm thickness over the contact surface between the module and the heat sink, which is also useful for preventing corrosion. Furthermore, the grease should be with stable quality and long-term endurance within wide operating temperature range. The contacting thermal resistance between DIIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

Pay attention to the selection of thermal conductive grease. The grease thickness after fixing the heatsink may increase due to the properties of the grease (contained filler diameter, viscosity, amount of application and so on). And it may cause increase of contact thermal resistance or package crack. Please contact thermal conductive grease manufacturer for its detailed characteristics.

Mini DIIPM with BSD Series APPLICATION NOTE

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
 (Note: The reflow soldering cannot be recommended for DIIPM.)

(1) Flow (wave) Soldering

DIIPM is tested on the condition described in Table 2-4-3 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-4-3 Reliability test specification

Item	Condition
Soldering thermostability	260±5°C, 10±1s

(2) Hand soldering

Since the temperature impressed upon the DIIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, the unambiguous hand soldering condition cannot be decided.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIIPM terminal should be kept under 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample: PSSxxS71F6

b. Evaluation procedure

- Put the soldering tip of 50W iron (temperature set to 400°C) on the terminal within 1mm from the toe.
- (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.

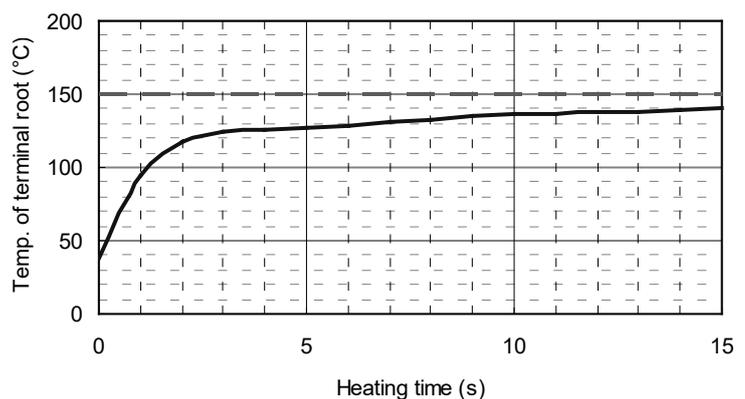
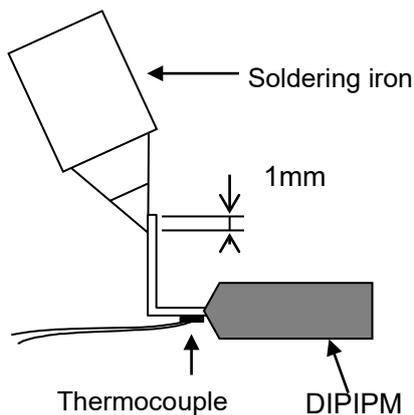


Fig.2-4-5 Heating and measuring point

Fig.2-4-6 Temperature alteration of the terminal root (Example)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

CHAPTER 3 SYSTEM APPLICATION GUIDANCE

3.1 Application Guidance

This chapter states the Mini DIIPM application method and interface circuit design hints.

3.1.1 System connection

- C1: Electrolytic type with good temperature and frequency characteristics.
Note: the capacitance also depends on the PWM control strategy of the application system
- C2: 0.22μ-2μF ceramic capacitor with good temperature, frequency and DC bias characteristics
- C3: 0.1μ-0.22μF Film capacitor (for snubber)
- D1: Zener diode 24V/1W for surge absorber

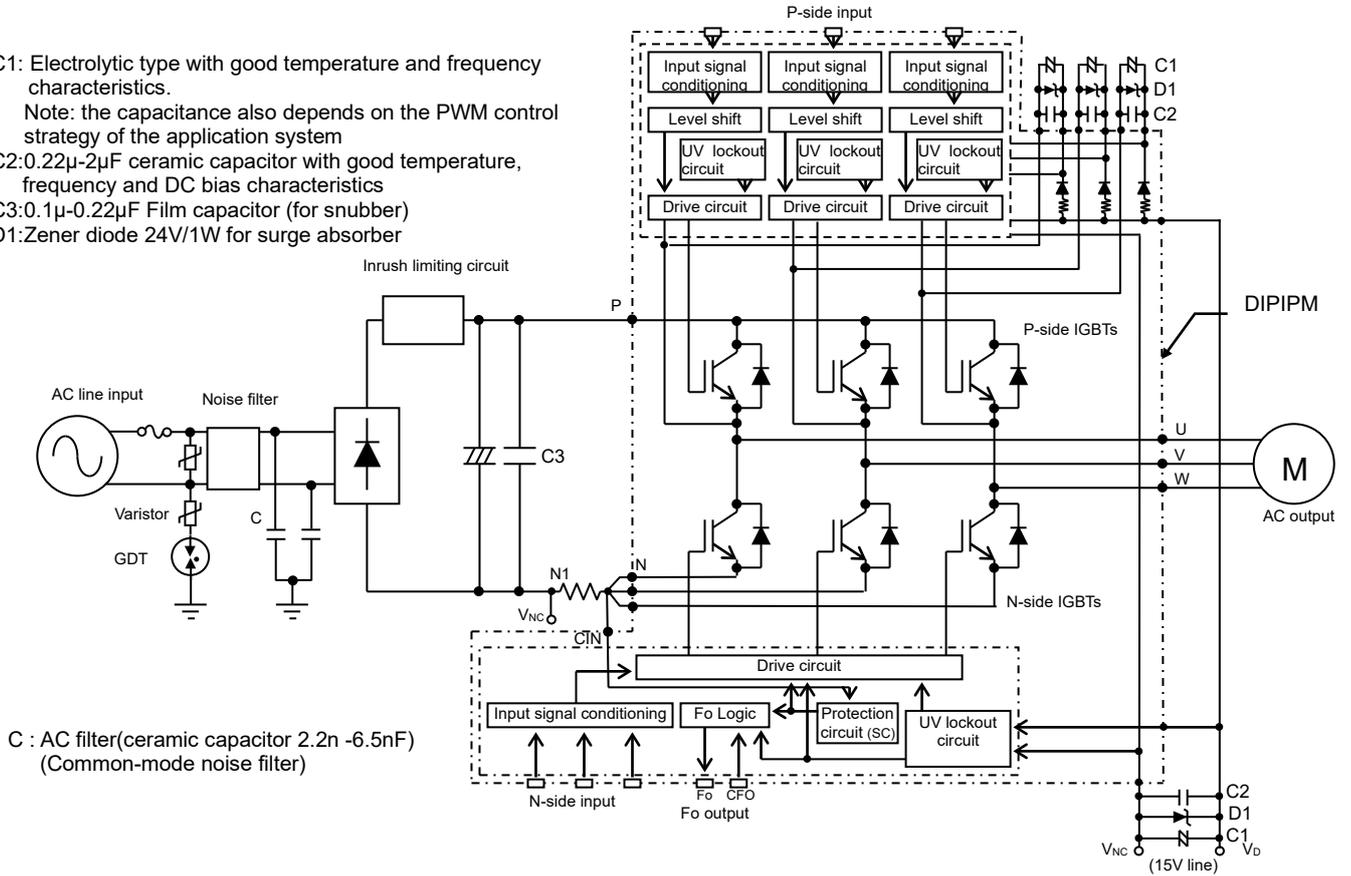


Fig.3-1-1 System block diagram (Example)

Mini DIIPM with BSD Series APPLICATION NOTE

3.1.3 Interface Circuit (Example of Opto-coupler Isolated Interface)

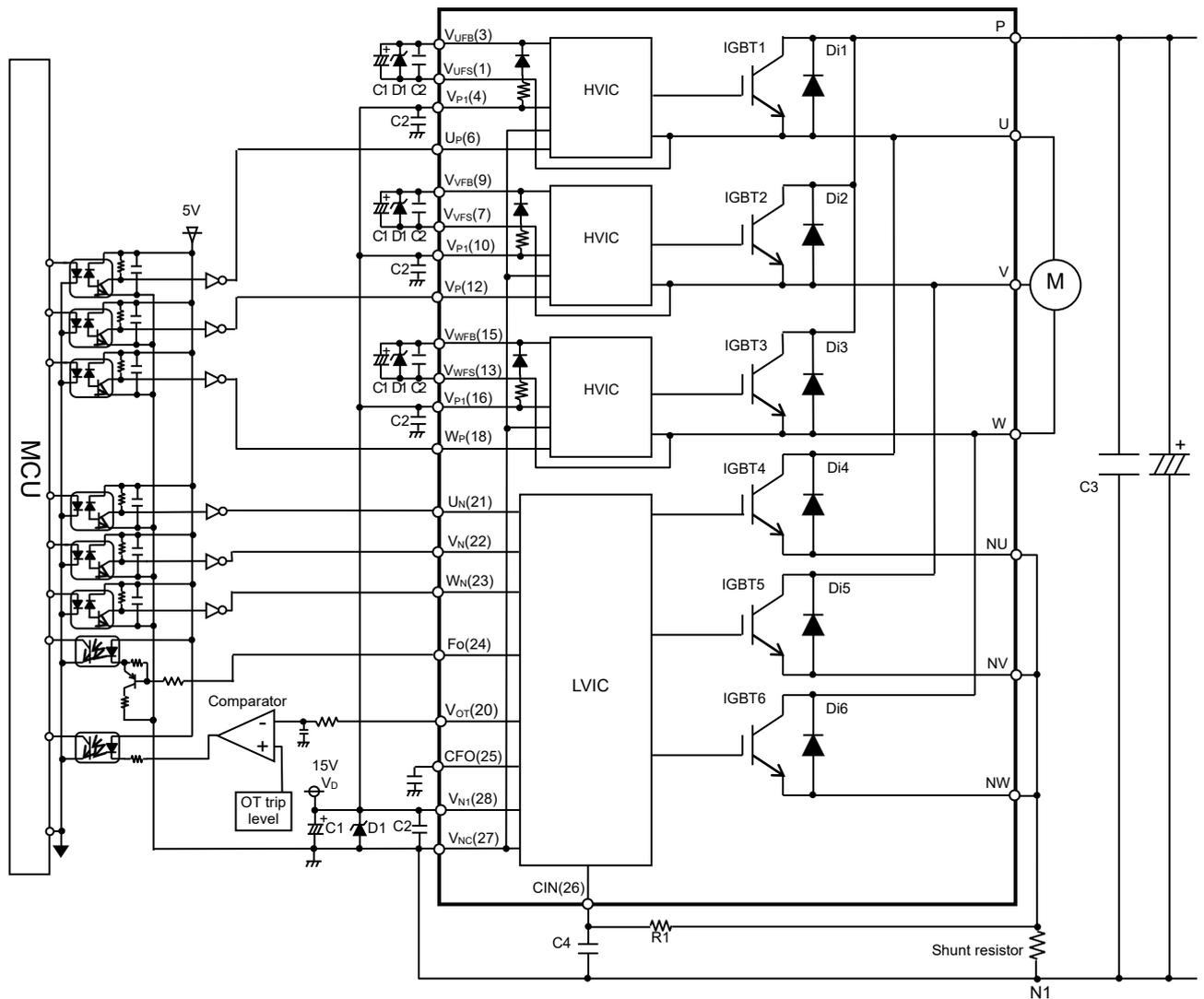


Fig.3-1-3 Interface circuit example with opto-coupler

Note:

- (1) High speed (high CMR) opto-coupler is recommended.
- (2) Fo terminal sink current for inverter part is max.1mA. It is recommended for driving coupler to apply buffer. To prevent Fo output from malfunctioning, it is recommended to make wiring from Fo terminal to buffer Tr and coupler as short as possible.
- (3) About comparator circuit at VOT output, it is recommended to design the input circuit with hysteresis because of preventing output chattering.

Mini DIIPM with BSD Series APPLICATION NOTE

3.1.4 External SC Protection Circuit with Using Three Shunt Resistors

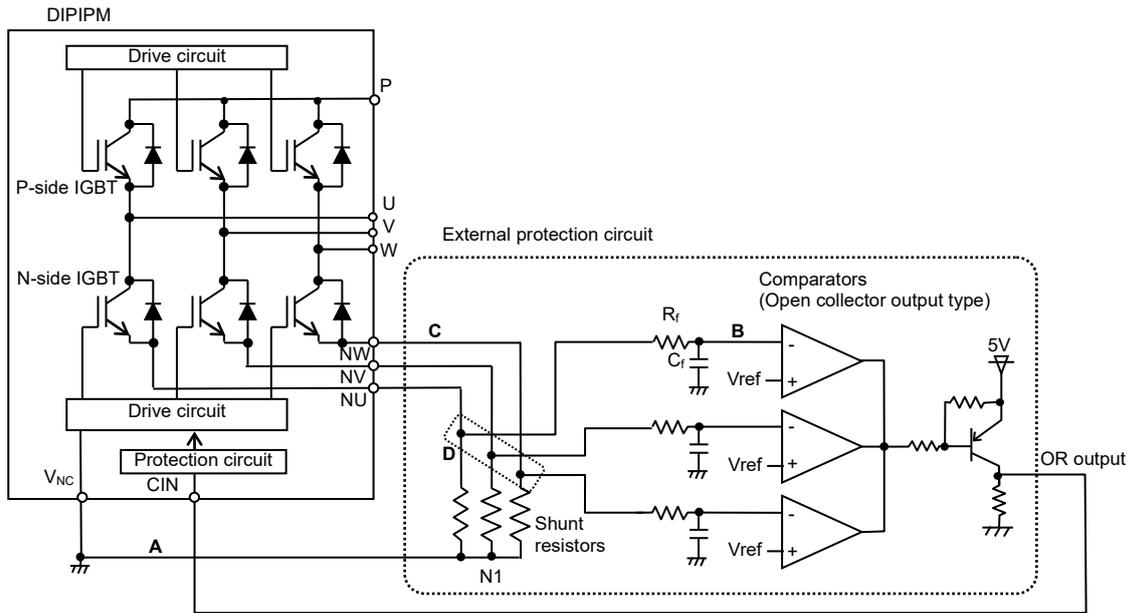


Fig.3-1-4 Interface circuit example

Note:

- (1) It is necessary to set the time constant $R_f C_f$ of external comparator input so that IGBT stop within $2\mu s$ when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
- (2) The threshold voltage V_{ref} should be set up the same rating of short circuit trip level ($V_{sc(ref)}$ typ. 0.48V).
- (3) Select the external shunt resistance so that SC trip-level is less than specified value.
- (4) To avoid malfunction, the wiring A, B, C should be as short as possible.
- (5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
- (6) OR output high level should be over 0.51V (=maximum $V_{sc(ref)}$).
- (7) GND of Comparator, GND of V_{ref} circuit and C_f should be not connected to power GND but to control GND wiring.

3.1.5 Circuits of Signal Input Terminals and Fo Terminal

(1) Internal Circuit of Control Input Terminals

DIIPM is high-active input logic. $3.3k\Omega$ (min) pull-down resistor is built-in each input circuits of the DIIPM as shown in Fig.3-1-5, so external pull-down resistor is not needed.

Furthermore, by lowering the turn on and turn off threshold value of input signal as shown in Table 3-1-1, a direct coupling to 3V class microcomputer or DSP becomes possible.

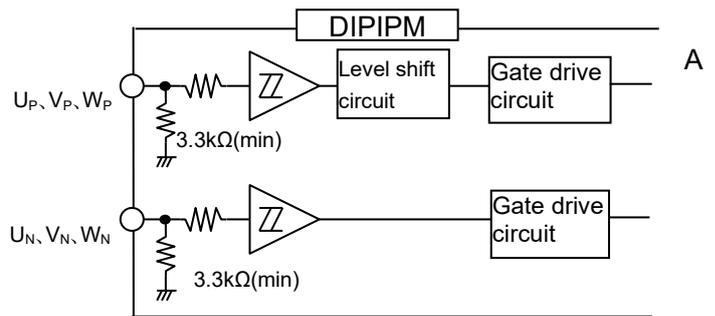


Fig.3-1-5 Internal structure of control input terminals

Table 3-1-1 Input threshold voltage ratings($T_j=25^\circ C$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	$V_{th(on)}$	$U_P, V_P, W_P - V_{NC}$ terminals $U_N, V_N, W_N - V_{NC}$ terminals	-	2.1	2.6	V
Turn-off threshold voltage	$V_{th(off)}$		0.8	1.3	-	
Threshold voltage hysteresis	$V_{th(hys)}$		0.35	0.8	-	

Note: The wiring of each input should be patterned as short as possible. And if the pattern is long and the noise is imposed on the pattern, it may be effective to insert RC filter. There are limits for the minimum input pulse width in the DIIPM. The DIIPM might make no response or delayed response, if the input pulse width (both on and off) is shorter than the specified value. (Table 3-1-2)

Mini DIPIPM with BSD Series APPLICATION NOTE

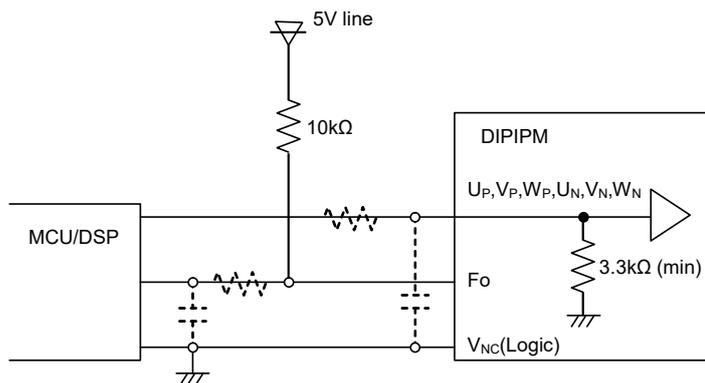


Fig.3-1-6 Control input connection

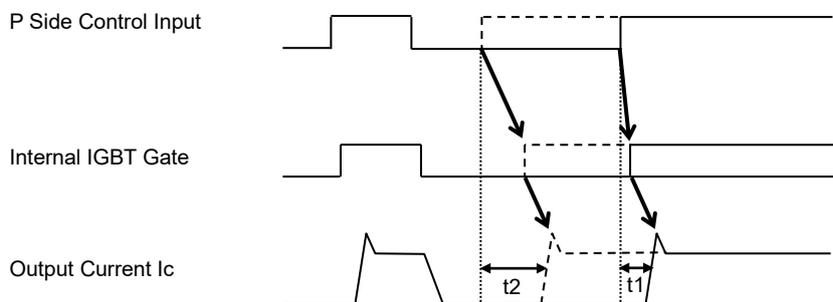
Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.

The DIPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Table 3-1-2 Allowable minimum input pulse width (Refer the datasheet for each product about detail)

		Condition		Part number	Min. value	Unit		
On signal	PWIN(on)	-		PSSxxS51F6	1.0	μs		
				PSSxxS71F6	0.7			
Off signal	PWIN(off)	$200 \leq V_{CC} \leq 350V$, $13.5 \leq V_D \leq 16.5V$, $13.5 \leq V_{DB} \leq 18.5V$, $-20 \leq T_C \leq 100^\circ C$, N line wiring inductance less than 10nH		Up to rated current			PSSxxS51F6	1.0
							PSS20S71F6	1.4
							PSS30S71F6	1.5
				From rated current to 1.7times of rated current			PSS50S71F6	1.5
							PSS20S71F6	2.5
							PSS30S71F6	3.0
				From 1.7 times to 2.0 times of rated current			PSS50S71F6	3.0
							PSS20S71F6	3.0
						PSS30S71F6	3.6	
PSS50S71F6	3.6							

*) Input signal with ON pulse width less than PWIN(on) might make no response. IPM might make no response or delayed response(PSSxxS71F6 only) for the input OFF signal with pulse width less than PWIN(off). (Delay occurs for p-side only.) Please refer below about delayed response.



Real line: off pulse width > PWIN(off); turn on time t1
 Broken line: off pulse width < PWIN(off); turn on time t2
 (t1: Normal switching time)

Fig.3-1-7 Delayed Response with shorter input off (P-side only)

Mini DIIPM with BSD Series APPLICATION NOTE

(2) Internal Circuit of Fo Terminal

F_o terminal is an open drain type, it should be pulled up to a 5V supply as shown in Fig.3-1-6. Fig.3-1-8 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 1mA. If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-1-2 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V _{FOH}	V _{SC} =0V, Fo=10kΩ, 5V pulled-up	4.9	-	-	V
	V _{FOL}	V _{SC} =1V, Fo=1mA	-	-	0.95	V

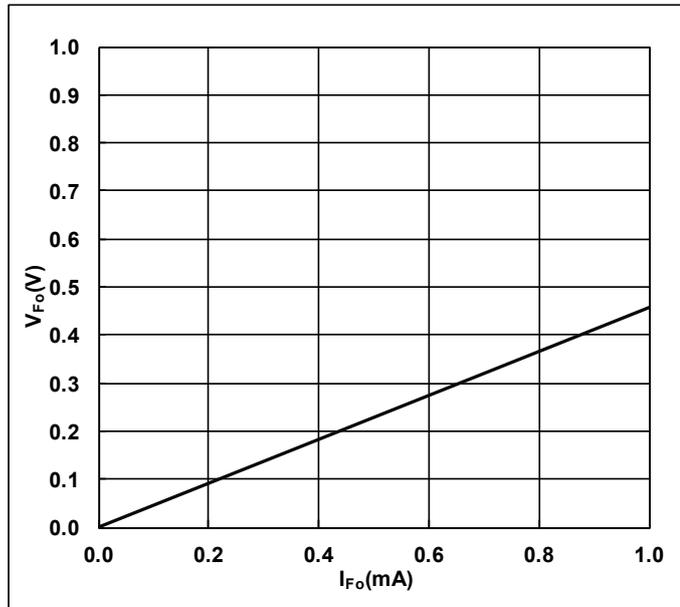


Fig.3-1-8 Fo terminal typical V-I characteristics (V_D=15V, T_J=25°C)

3.1.6 Snubber Circuit

In order to prevent DIIPM from destruction by extra surge, the wiring length between the smoothing capacitor and P terminal (DIIPM) – N1 points (shunt resistor terminal) should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted in the DC-link and near to P, N1.

Normally there are two positions ((1) or (2)) to mount a snubber capacitor as shown in Fig.3-1-9. Snubber capacitor should be installed in the position (2) so as to suppress surge voltage effectively. However, the charging and discharging currents generated by the wiring inductance and the snubber capacitor will flow through the shunt resistor, which might cause erroneous protection if this current is large enough.

In order to suppress the surge voltage maximally, the wiring at part-A (including shunt resistor parasitic inductance) should be as small as possible. A better wiring example is shown in location (3).

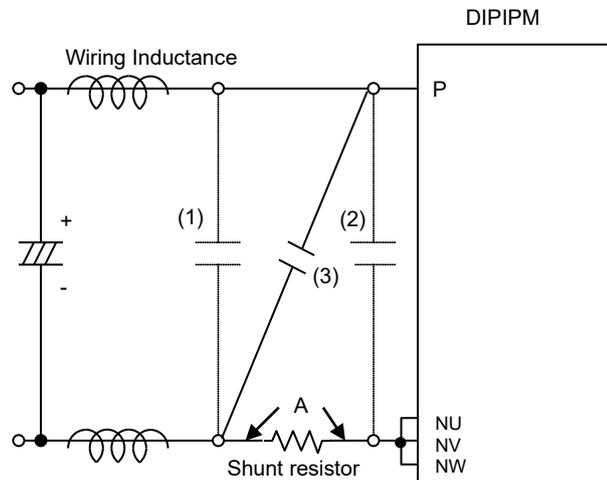


Fig.3-1-9 Recommended snubber circuit location

Mini DIIPM with BSD Series APPLICATION NOTE

3.1.7 Recommended Wiring Method around Shunt Resistor

External shunt resistor is employed to detect short-circuit accident. A longer wiring between the shunt resistor and DIIPM causes so much large surge that might damage built-in IC. To decrease the pattern inductance, the wiring between the shunt resistor and DIIPM should be as short as possible and using low inductance type resistor such as SMD resistor instead of long-lead type resistor.

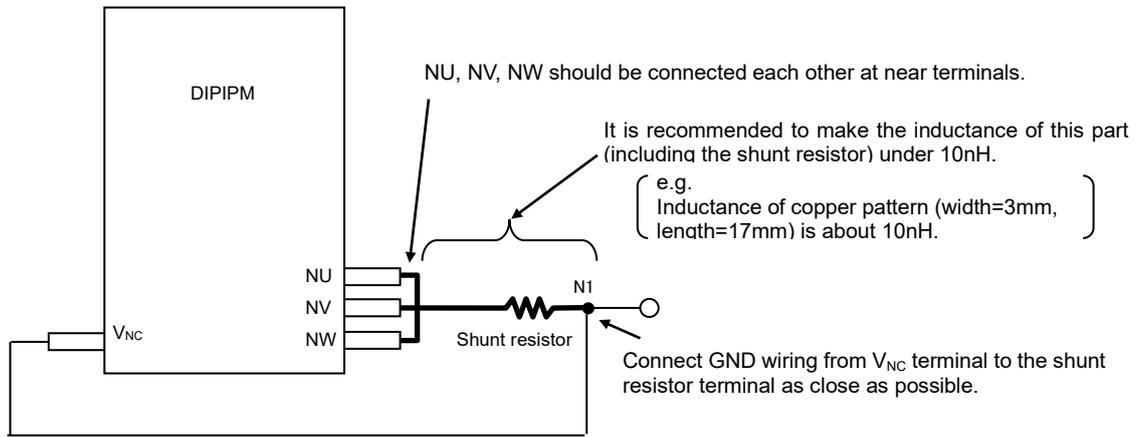


Fig.3-1-10 Wiring instruction (In the case of using with one shunt resistor)

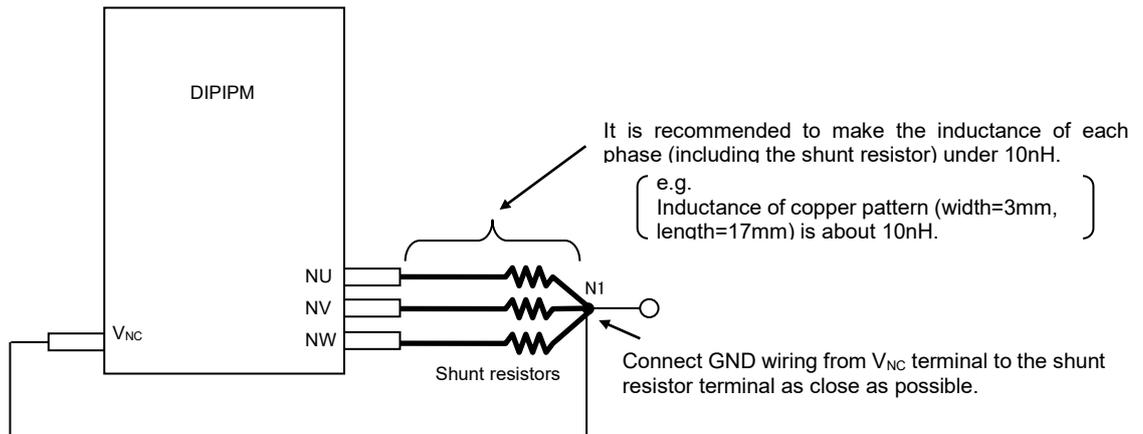


Fig.3-1-11 Wiring instruction (In the case of using with three shunt resistors)

Mini DIIPM with BSD Series APPLICATION NOTE

Influence of pattern wiring around the shunt resistor is shown below.

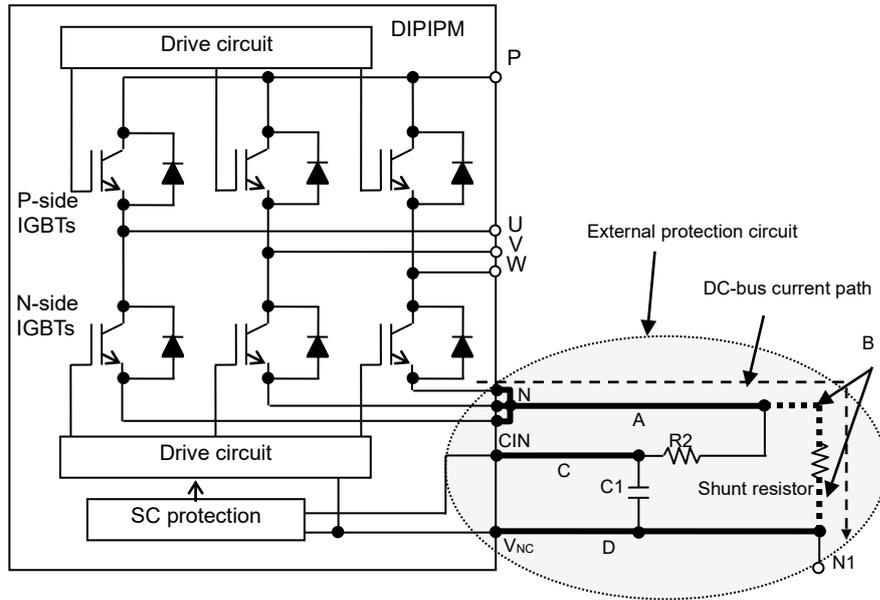


Fig.3-1-12 External protection circuit

(1) Influence of the part-A wiring

The ground of N-side IGBT gate is V_{NC} . If part-A wiring pattern in Fig.3-1-11 is too long, extra voltage generated by the wiring parasitic inductance will result the potential of IGBT emitter variation during switching operation. Please install shunt resistor as close to the N terminal as possible.

(2) Influence of the part-B wiring

The part-B wiring affects SC protection level. SC protection works by detecting the voltage of the CIN terminals. If part-B wiring is too long, extra surge voltage generated by the wiring inductance will lead to deterioration of SC protection level. It is necessary to connect CIN and V_{NC} terminals directly to the two ends of shunt resistor and avoid long wiring.

(3) Influence of the part-C wiring pattern

C1R2 filter is added to remove noise influence occurring on shunt resistor. Filter effect will dropdown and noise will easily superimpose on the wiring if part-C wiring is too long. It is necessary to install the C1R2 filter near CIN, V_{NC} terminals as close as possible.

(4) Influence of the part-D wiring pattern

Part-D wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected.

Mini DIIPM with BSD Series APPLICATION NOTE

3.1.8 Precaution for Wiring on PCB

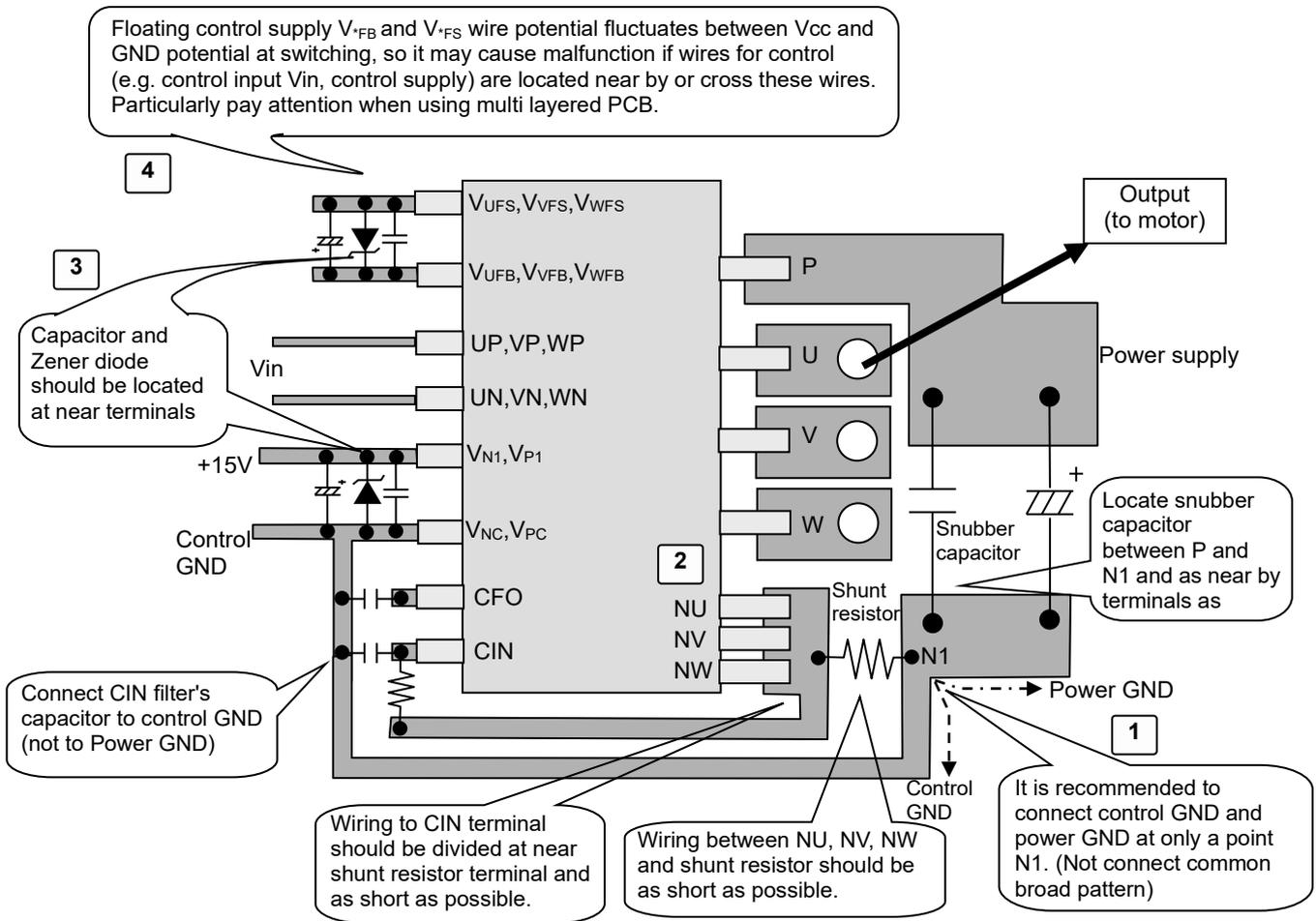


Fig.3-1-13 Precaution for wiring on PCB

The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. It causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Then the arm short might occur.
	•Ground loop pattern exists.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short might occur.
2	•Large inductance of wiring between N and N1 terminal	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction due to VS voltage (output terminal potential) dropping excessively. •LVIC surge destruction
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction might occur.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	Cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIIPM. Then incorrect signals are input to DIIPM input, and arm short (short circuit) might occur.

Mini DIIPM with BSD Series APPLICATION NOTE

3.1.9 Parallel operation of DIIPM

Fig.3-1-14 shows the circuitry of parallel connection of two DIIPMs. Route (1) and (2) indicate the gate charging path of low-side IGBT in DIIPM No.1 & 2 respectively. In the case of DIIPM 1, the parasitic inductance becomes large by long wiring and it might have a negative effect on DIIPM's switching operation. (Chare operation of bootstrap capacitor for high-side might be affected too.) Also, such a wiring makes DIIPM be affected by noise easily, then it might lead to malfunction. If more DIIPMs are connected in parallel, GND pattern becomes longer and the influence to other circuit (protection circuit etc.) by the fluctuation of GND potential is conceivable, therefore parallel connection is not recommended.

Because DIIPM doesn't consider the fluctuation of characteristics between each phase definitely, it cannot be recommended to drive same load by parallel connection with other phase IGBT or IGBT of other DIIPM.

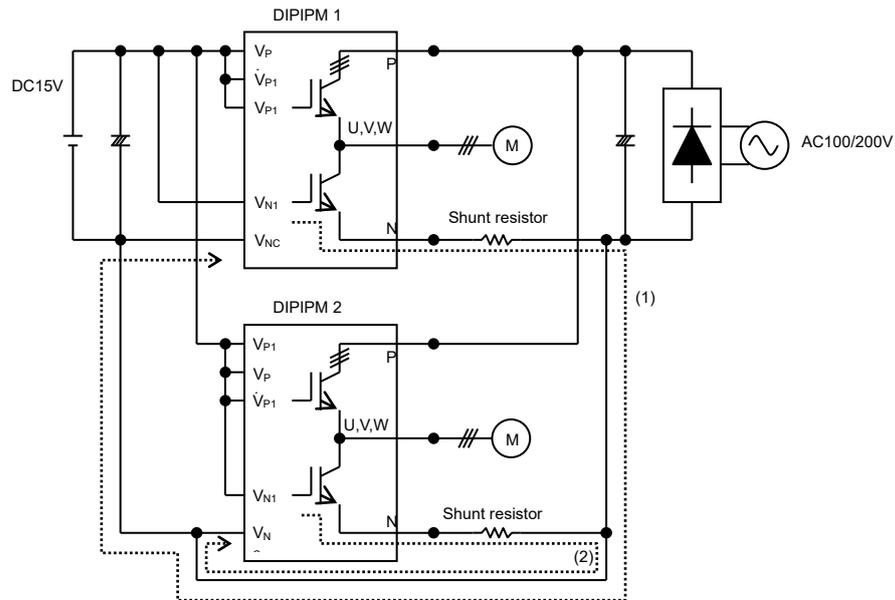


Fig.3-1-14 Parallel operation

3.1.10 SOA of Mini DIIPM

The following describes the SOA (Safety Operating Area) of the Mini DIIPM.

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : Supply voltage applied on P-N terminals

$V_{CC(surge)}$: Total amount of V_{CC} and surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{CC(prot)}$: DC-link voltage that DIIPM can protect itself.

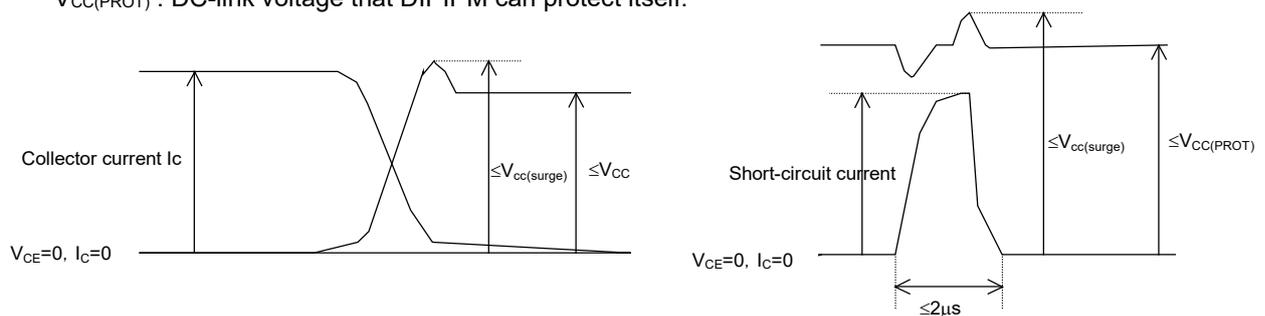


Fig.3-1-15 SOA at switching mode and short-circuit mode

In case of Switching

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIIPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC} , that is 450V.

In case of Short-circuit

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIIPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC} , that is, 400V.

Mini DIIPM with BSD Series APPLICATION NOTE

3.1.11 SCSOA

Fig.3-1-16~22 show the typical SCSOA performance curves of each products.

(Conditions: $V_{cc}=400V$, $T_j=125^{\circ}C$ at initial state, $V_{cc}(\text{surge})\leq 500V$ (surge included), non-repetitive, 2m load.)

In the case of PSS20S71F6, it can shutdown safely an SC current that is about 8 times of its current rating under the conditions if the IGBT conducting period is less than about $4.5\mu s$. Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.

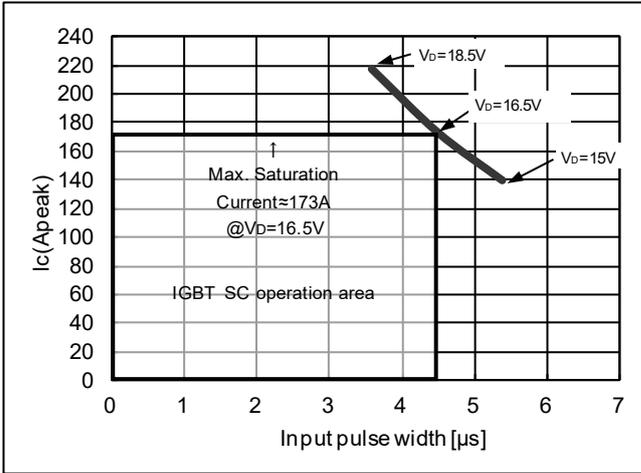


Fig.3-1-16 Typical SCSOA curve of PSS20S71F6

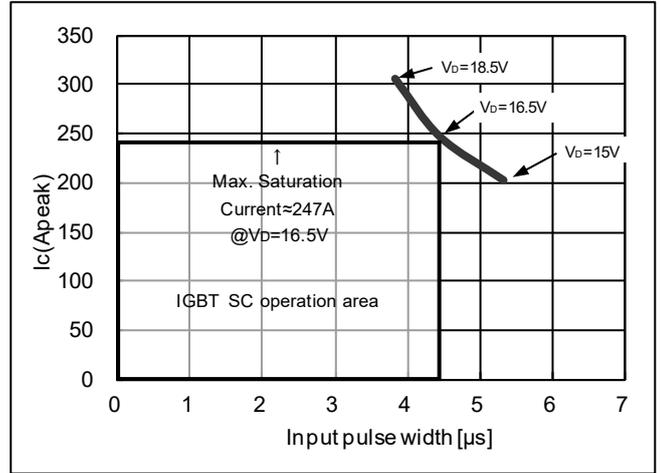


Fig.3-1-17 Typical SCSOA curve of PSS30S71F6

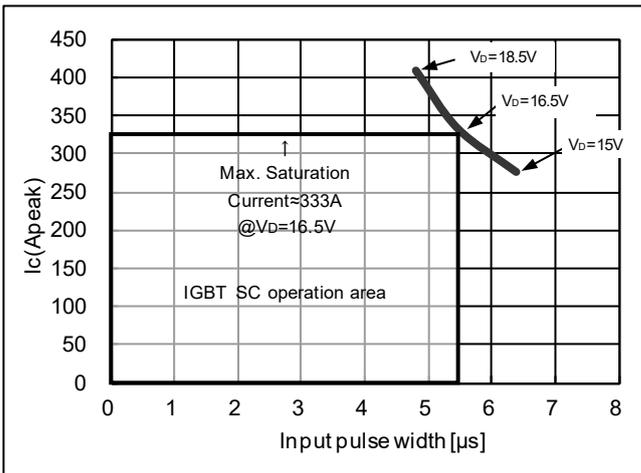


Fig.3-1-18 Typical SCSOA curve of PSS50S71F6

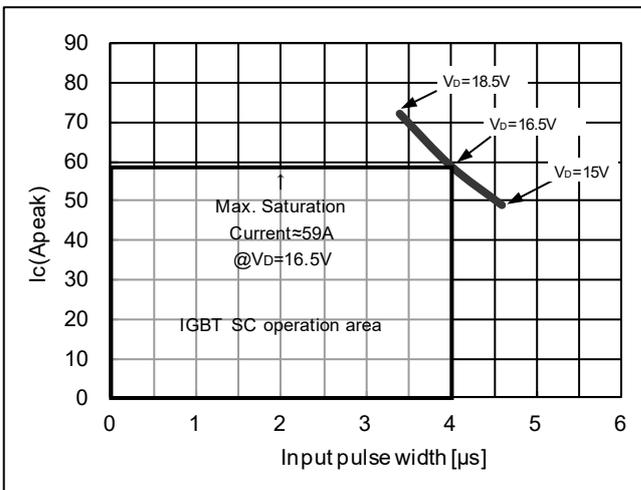


Fig.3-1-19 Typical SCSOA curve of PSS05S51F6

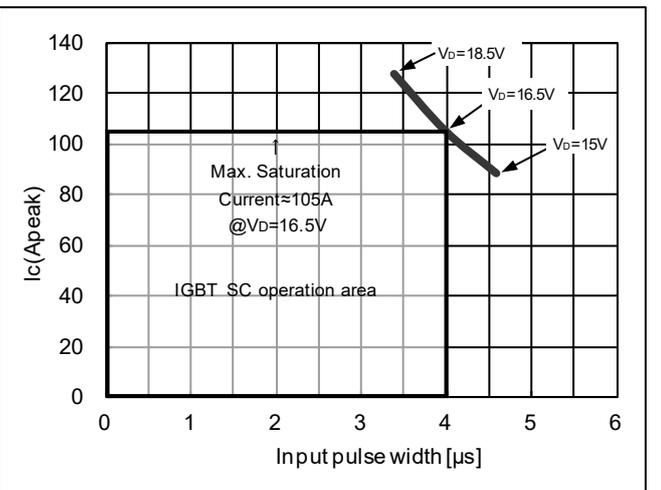


Fig.3-1-20 Typical SCSOA curve of PSS10S51F6

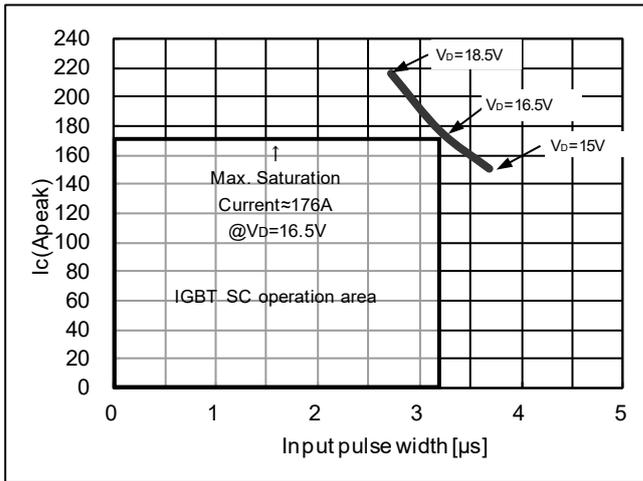


Fig.3-1-21 Typical SCSOA curve of PSS15S51F6

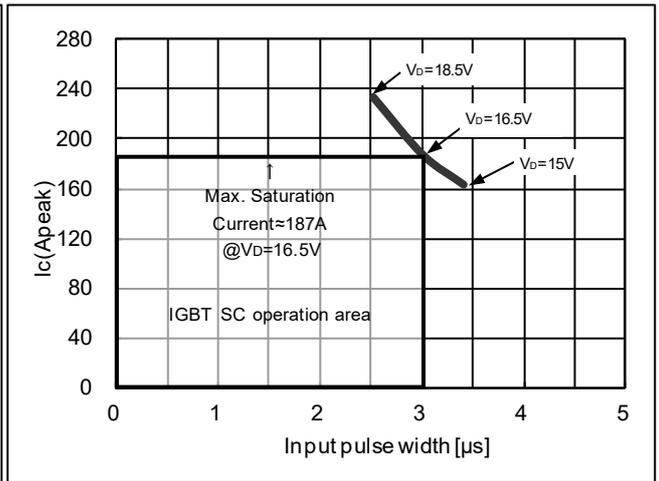


Fig.3-1-22 Typical SCSOA curve of PSS20S51F6

3.1.12 Power Life Cycles

When DIIPM is in operation, repetitive temperature variation will happen on the IGBT junctions (ΔT_j). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-1-23 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔT_j). (The curve is a regression curve based on 3 points of $\Delta T_j=46, 88, 98K$ with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

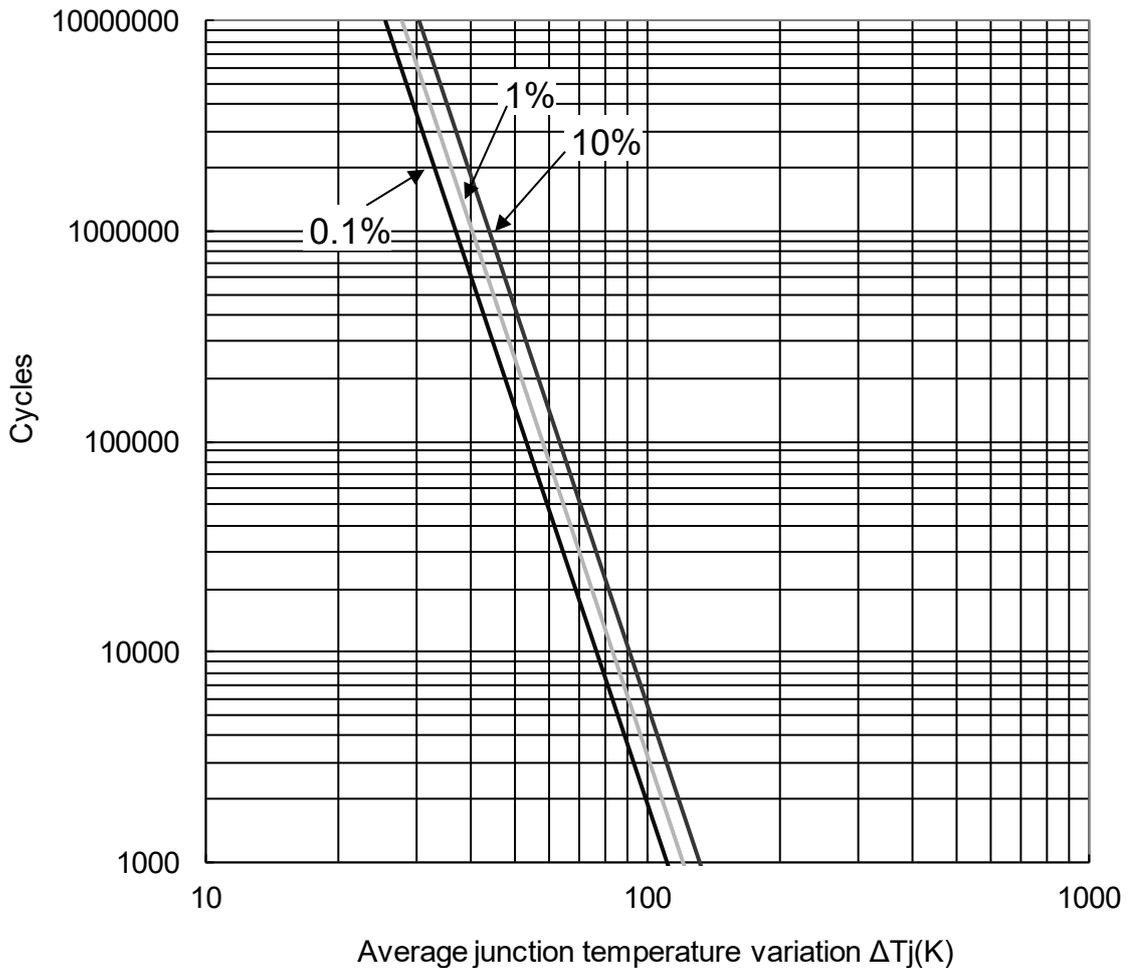


Fig.3-1-23 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

- Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

- Assumptions

- (1) PWM controlled VVVF inverter with sinusoidal output;
- (2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
- (3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
- (4) Output current varies with $I_{cp} \cdot \sin x$ and it does not include ripple.
- (5) Power factor of load output current is $\cos \theta$, ideal inductive load is used for switching.

- Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+D \times \sin x}{2}$ which is equivalent to the output voltage variation. From the power factor $\cos \theta$, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$\begin{aligned} \text{Output current} &= I_{cp} \times \sin x \\ \text{PWM Duty} &= \frac{1 + D \times \sin(x + \theta)}{2} \end{aligned}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$\begin{aligned} V_{ce(sat)} &= V_{ce(sat)}(@ I_{cp} \times \sin x) \\ V_{ec} &= (-1) \times V_{ec}(@ I_{cp} (= I_{cp}) \times \sin x) \end{aligned}$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi} \int_0^\pi (I_{cp} \times \sin x) \times V_{ce(sat)}(@ I_{cp} \times \sin x) \times \frac{1 + D \sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi} \int_\pi^{2\pi} ((-1) \times I_{cp} \times \sin x) ((-1) \times V_{ec}(@ I_{cp} \times \sin x)) \times \frac{1 + D \sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi} \int_0^\pi (P_{sw(on)}(@ I_{cp} \times \sin x) + P_{sw(off)}(@ I_{cp} \times \sin x)) \times fc \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-2-1, and its dynamic loss can be calculated by the following expression:

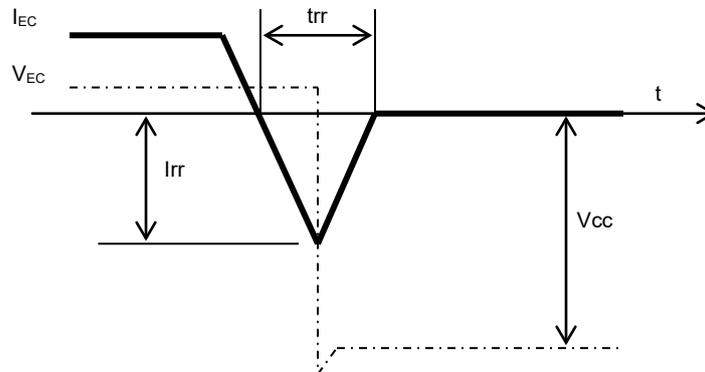


Fig.3-2-1 Ideal FWDi recovery characteristics curve

$$P_{SW} = \frac{I_{rr} \times V_{cc} \times t_{rr}}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\begin{aligned} & \frac{1}{2} \int_{\pi}^{2\pi} \frac{I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times t_{rr}(@ I_{cp} \times \sin x)}{4} \times fc \cdot dx \\ & = \frac{1}{8} \int_{\rho}^{2\pi} I_{rr}(@ I_{cp} \times \sin x) \times V_{cc} \times t_{rr}(@ I_{cp} \times \sin x) \times fc \cdot dx \end{aligned}$$

- Attention of applying the power loss simulation for inverter designs
 - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC} , and P_{sw} corresponding to the output current. The worst condition is most important.
 - PWM duty depends on the signal generating way.
 - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
 - $V_{CE(sat)}$, V_{EC} and $P_{sw}(on, off)$ should be the values at $T_j=125^{\circ}C$.

Mini DIIPM with BSD Series APPLICATION NOTE

3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-2-2 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: $V_{CC}=300V$, $V_D=V_{DB}=15V$, $V_{CE(sat)}=Typ.$, Switching loss=Typ., $T_j=125^\circ C$, $T_f=100^\circ C$, $\Delta T(j-f)=25K$ $R_{th(j-c)}=Max.$, $R_{th(c-f)}=0.3^\circ C/W$ (per 1/6 module), $P.F=0.8$, 3-phase PWM modulation, 60Hz sine waveform output

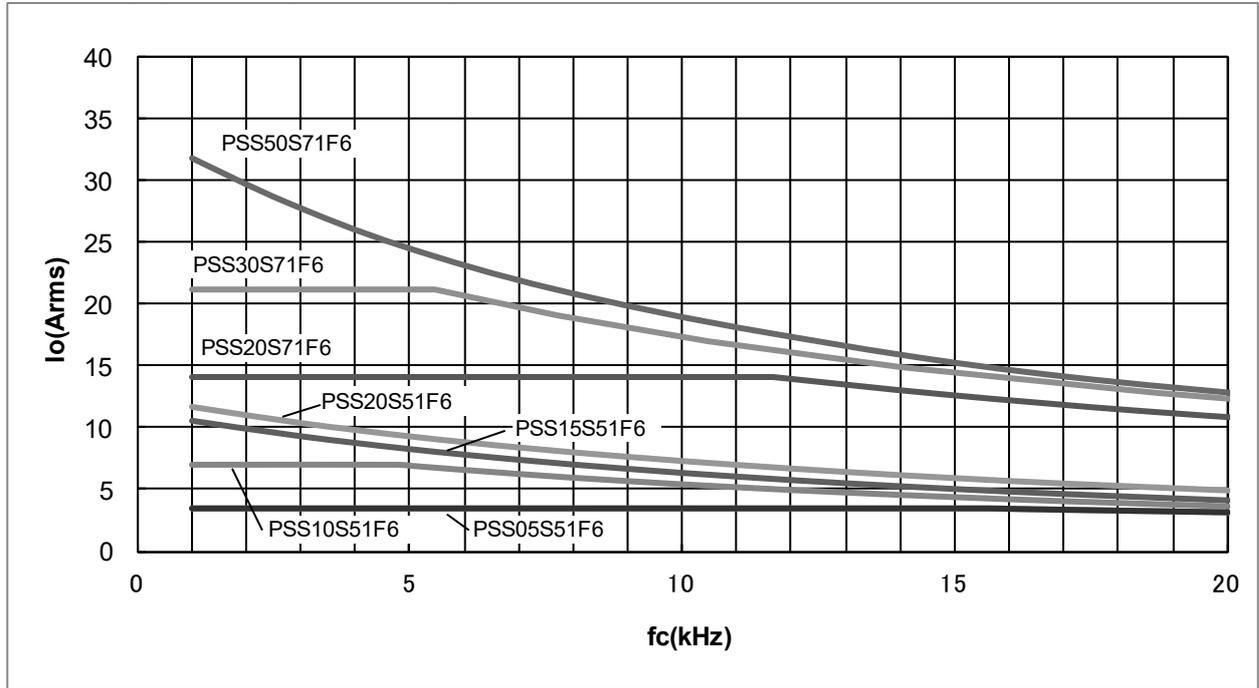


Fig.3-2-2 Effective current-carrier frequency characteristics

Fig.3-2-2 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition ($T_f=100^\circ C$, $T_j=125^\circ C$). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The inverter loss can be calculated by the free power loss simulation software is uploaded to the web site. URL: <http://www.MitsubishiElectric.com/semiconductors/>

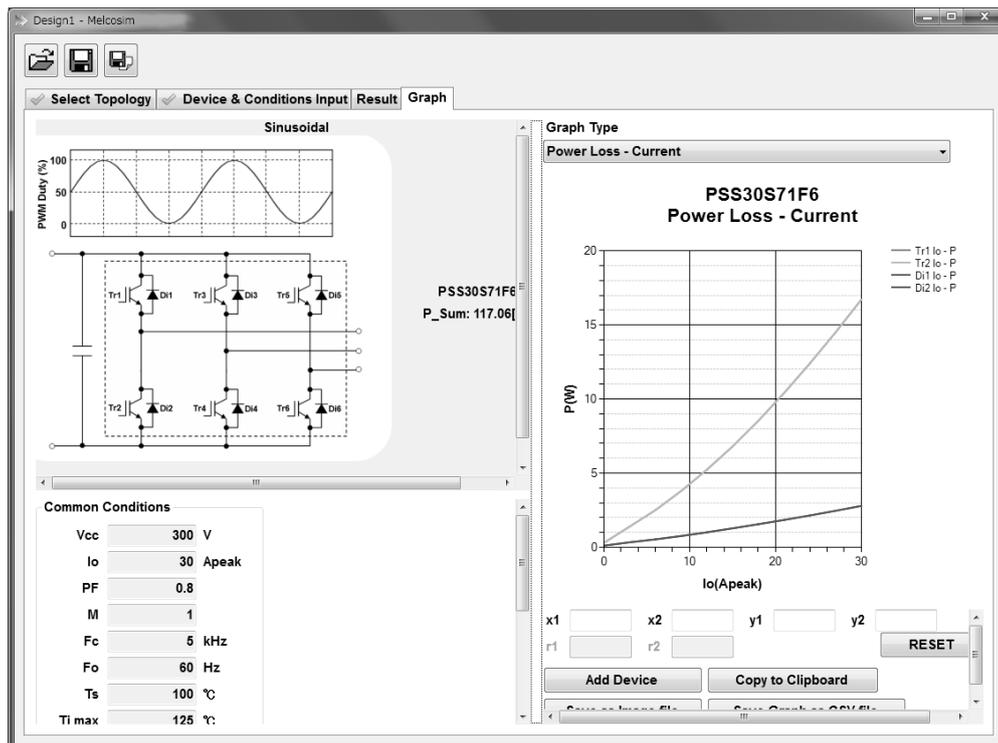


Fig.3-2-3 Loss simulator screen image

Mini DIIPM with BSD Series APPLICATION NOTE

3.3.3 Static Electricity Withstand Capability

DIIPM has been confirmed to be with typical +/-200V or more withstand capability against static electricity from the following tests shown in Fig.3-3-3, 4. The results (typical data) are described in Table 3-3-1.

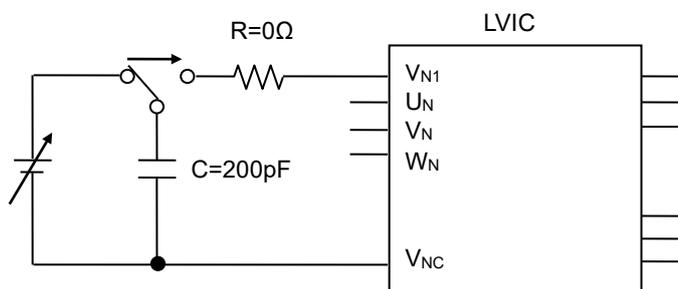


Fig.3-3-3 LVIC terminal Surge Test circuit

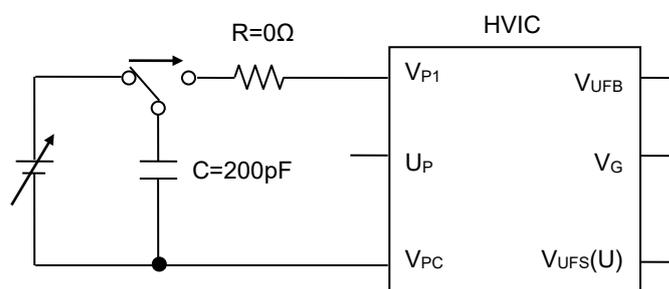


Fig.3-3-4 HVIC terminal Surge Test circuit

Conditions: Surge voltage is increased by 0.1kV step and only one surge pulse is impressed at each voltage. (Limit voltage of surge simulator: ±4.0kV, Judgment method; change in V-I characteristic)

Table 3-3-1 PSSxxS71F6 Typical ESD capability

[Control terminal part] Common data for PSSxxS71F6 because of all types have same interface circuit.

Terminals	+	-
UP, VP, WP-V _{NC}	1.0	1.1
V _{P1} - V _{NC}	1.7	1.8
V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}	4.0 or more	4.0 or more
UN, VN, WN-V _{NC}	1.1	1.0
V _{N1} -V _{NC}	4.0 or more	4.0 or more
CIN-V _{NC}	1.0	0.5
FO-V _{NC}	1.0	0.9
CFO-V _{NC}	0.9	1.0
V _{OT} -V _{NC}	1.1	1.4

[Power terminal part]

PSS20S71F6

Terminals	+	-
P-NU,NV,NW	3.0	4.0 or more
U-NU, V-NV, W-NW	3.0	4.0

PSS30S71F6

Terminals	+	-
P-NU,NV,NW	3.5	4.0 or more
U-NU, V-NV, W-NW	3.1	4.0 or more

PSS50S71F6

Terminals	+	-
P-NU,NV,NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

Mini DIIPM with BSD Series APPLICATION NOTE

Table 3-3-2 PSSxxS51F6 Typical ESD capability

[Control terminal part] Common data for PSSxxS71F6 because of all types have same interface circuit.

Terminals	+	-
UP, VP, WP-V _{NC}	0.8	1.1
V _{P1} - V _{NC}	1.2	1.3
V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}	3.3	3.4
UN, VN, WN-V _{NC}	1.0	0.6
V _{N1} -V _{NC}	3.9	2.9
CIN-V _{NC}	0.8	0.7
FO-V _{NC}	0.5	0.9
CFO-V _{NC}	0.7	1.1
V _{OT} -V _{NC}	0.8	1.3

[Power terminal part]

PSS05S51F6

Terminals	+	-
P-NU,NV,NW	4.0	3.4
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

PSS10S51F6

Terminals	+	-
P-NU,NV,NW	3.5	3.8
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

PSS15S51F6

Terminals	+	-
P-NU,NV,NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

PSS20S51F6

Terminals	+	-
P-NU,NV,NW	4.0 or more	4.0 or more
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

CHAPTER 4 Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor. (Mini DIIPM with BSD series integrates BSD and limiting resistor and can make bootstrap circuit by adding outer BSC only.) It uses the BSC as a control supply for driving P-side IGBT. The BSC supplies gate charge when P-side IGBT turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-1-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side IGBT increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIIPM application note "*Bootstrap Circuit Design Manual*"

The BSD characteristics for Mini DIIPM with BSD series and the circuit current characteristics in switching situation of P-side IGBT are described as below.

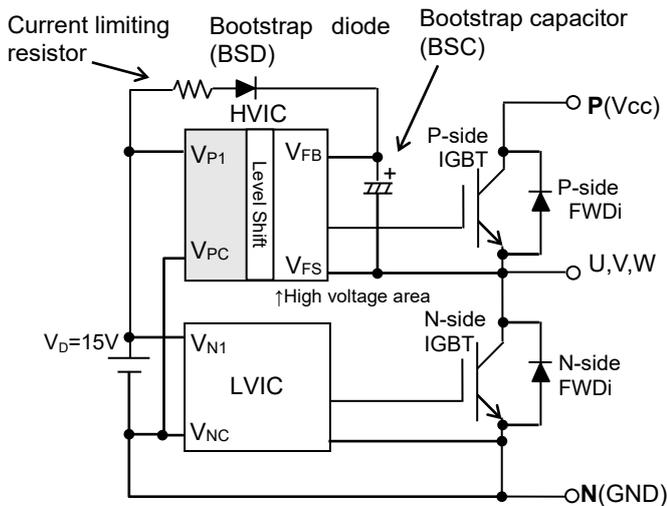


Fig.4-1-1 Bootstrap Circuit Diagram

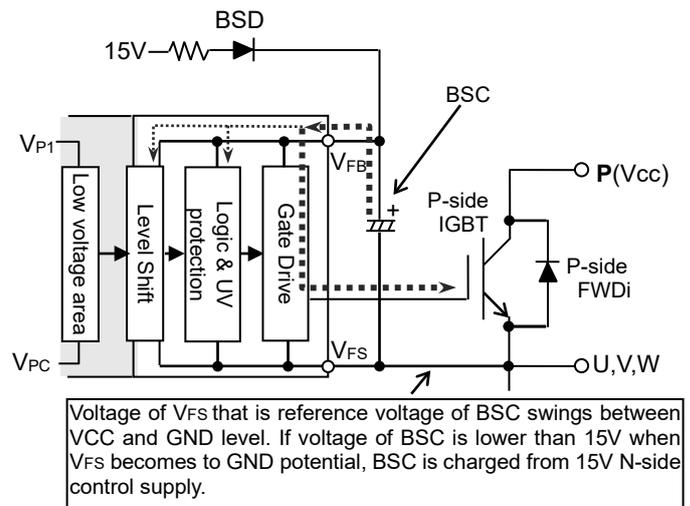


Fig.4-1-2 Bootstrap Circuit Diagram

4.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current I_{DB} at steady state is maximum 0.55mA. But at switching state, because gate charge and discharge are repeated by switching, the circuit current exceeds 0.55mA and increases proportional to carrier frequency. For reference, Fig.4-2-1~7 show typical I_{DB} -carrier frequency f_c characteristics for PSSxxS71F6 and PSSxxS51F6.

(Conditions: $V_D=V_{DB}=15V$, $T_j=125^\circ C$ at which I_{DB} becomes larger, IGBT ON Duty=10, 30, 50, 70, 90%)

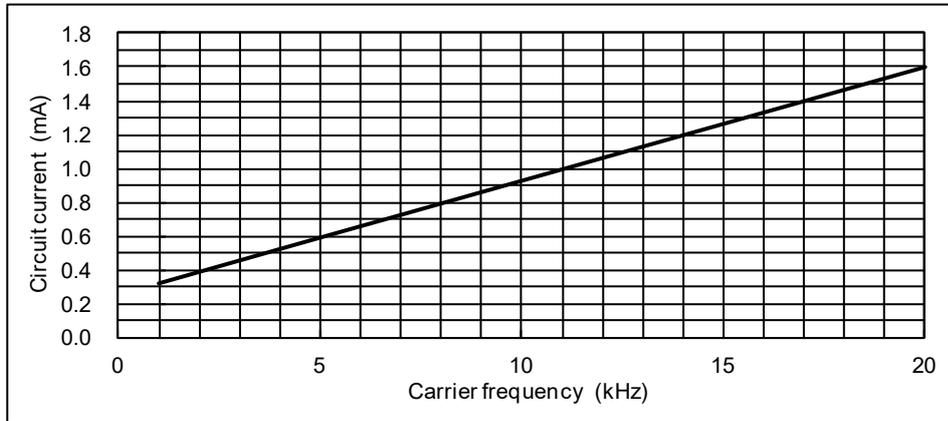


Fig.4-2-1 I_{DB} vs. Carrier frequency for PSS20S71F6

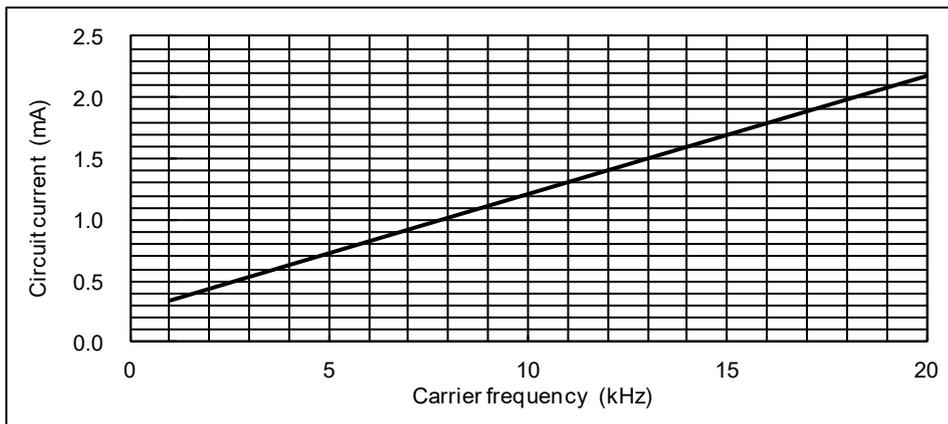


Fig.4-2-2 I_{DB} vs. Carrier frequency for PSS30S71F6

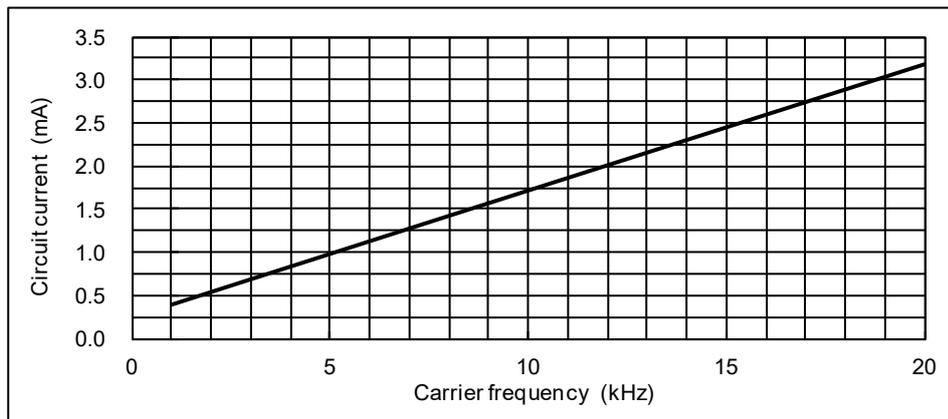


Fig.4-2-3 I_{DB} vs. Carrier frequency for PSS50S71F6

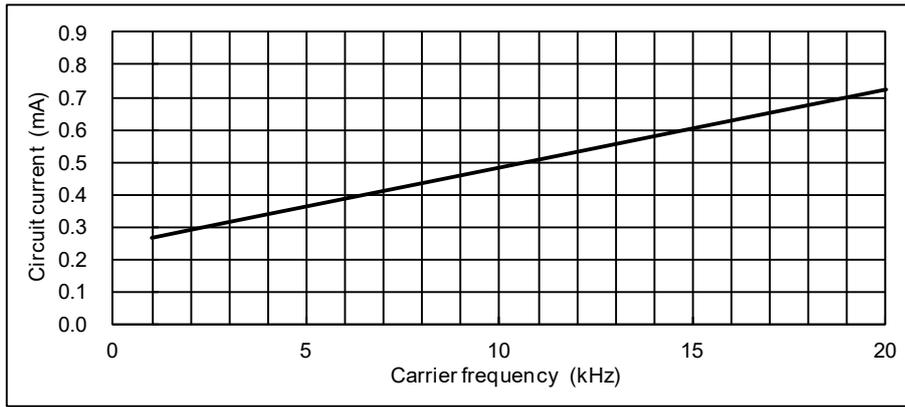


Fig.4-2-4 I_{DB} vs. Carrier frequency for PSS05S51F6 (5A/600V))

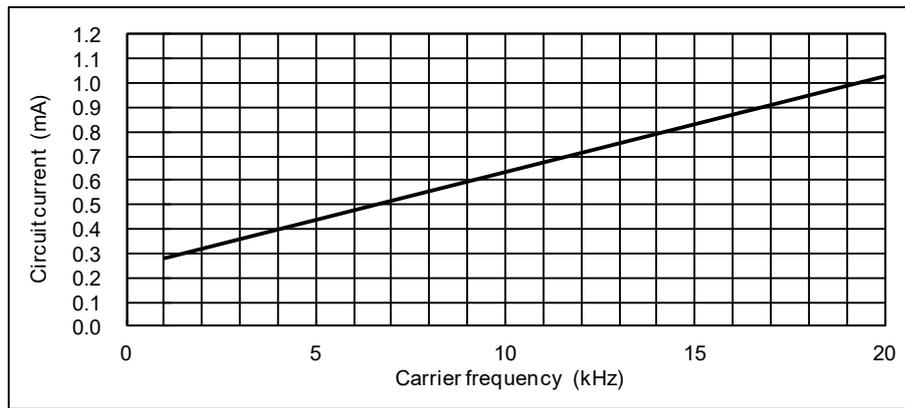


Fig.4-2-5 I_{DB} vs. Carrier frequency for PSS10S51F6 (10A/600V))

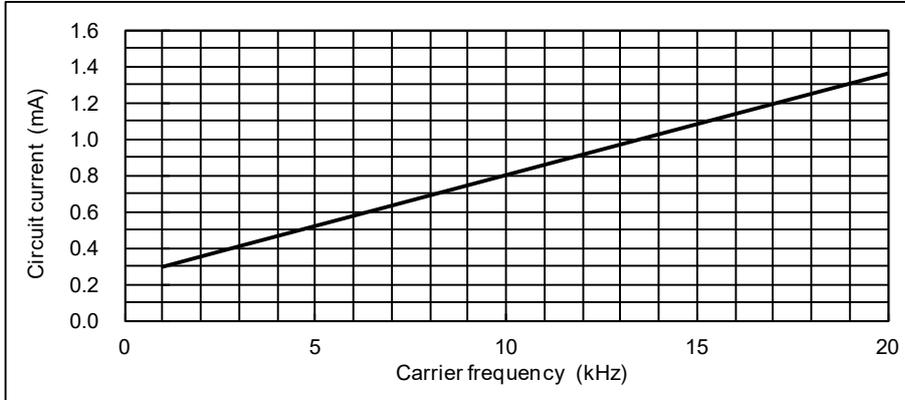


Fig.4-2-6 I_{DB} vs. Carrier frequency for PSS15S51F6 (15A/600V))

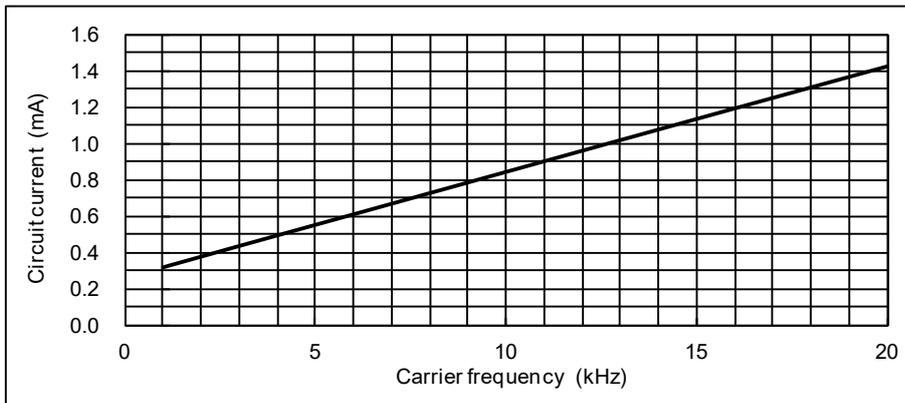


Fig.4-2-7 I_{DB} vs. Carrier frequency for PSS20S51F6 (20A/600V))

4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIIPM application note "*Bootstrap Circuit Design Manual*"

(1) Bootstrap capacitor

Electrolytic capacitors are used for BSC generally. And recently ceramic capacitors with large capacitance are also applied. But DC bias characteristic of the ceramic capacitor when applying DC voltage is considerably different from that of electrolytic capacitor. (Especially large capacitance type) Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-3-1.

Table 4-3-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta: -20~ 85°C)	<ul style="list-style-type: none"> Aluminum type: Low temp.: -10% High temp: +10% Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10% 	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on -70%~-15%

DC bias characteristic of electrolytic capacitor is not matter. But it is necessary to note ripple capability by repetitive charge and discharge, life time which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode

Mini DIIPM integrates bootstrap diodes for P-side driving supply. This BSD incorporates current limiting resistor (typ. 20Ω). The V_F - I_F characteristics (including voltage drop by built-in current limiting resistor) is shown in Fig.4-3-1 and Table 4-3-2.

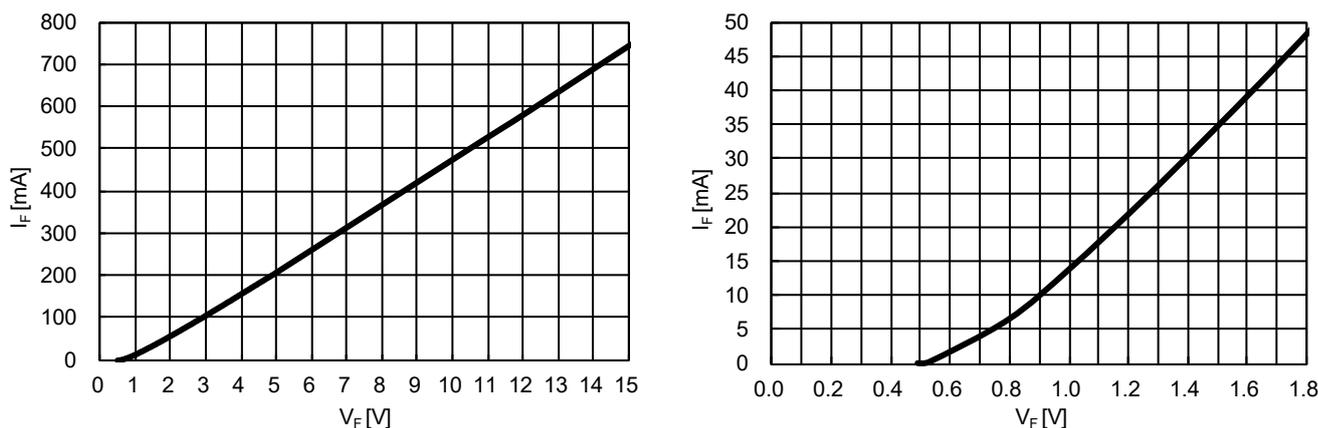


Fig.4-3-1 V_F - I_F curve for bootstrap Diode (The right figure is enlarged view)

Table 4-3-2 Electric characteristics of built-in bootstrap diode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Bootstrap Di forward voltage	V_F	$I_F=10mA$ including voltage drop by limiting resistor	0.5	0.9	1.3	V
Built-in limiting resistance	R	Included in bootstrap Di	16	20	24	Ω

4.4 Initial charging in bootstrap circuit

In the case of applying bootstrap circuit, it is necessary to charge to the BSC initially because voltage of BSC is 0V at initial state or it may go down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side IGBT normally. When outer load (e.g. motor) is connected to the DIIPM, BSC charging may be performed by turning on only one phase N-side IGBT since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restriction like control supply capability and so on.

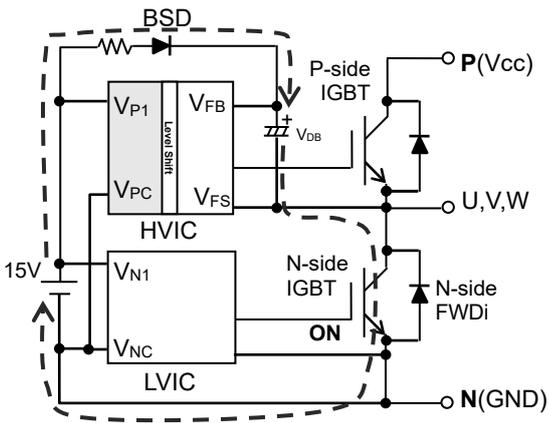


Fig.4-4-1 Initial charging root

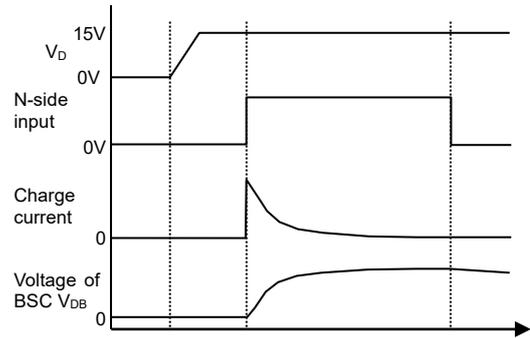


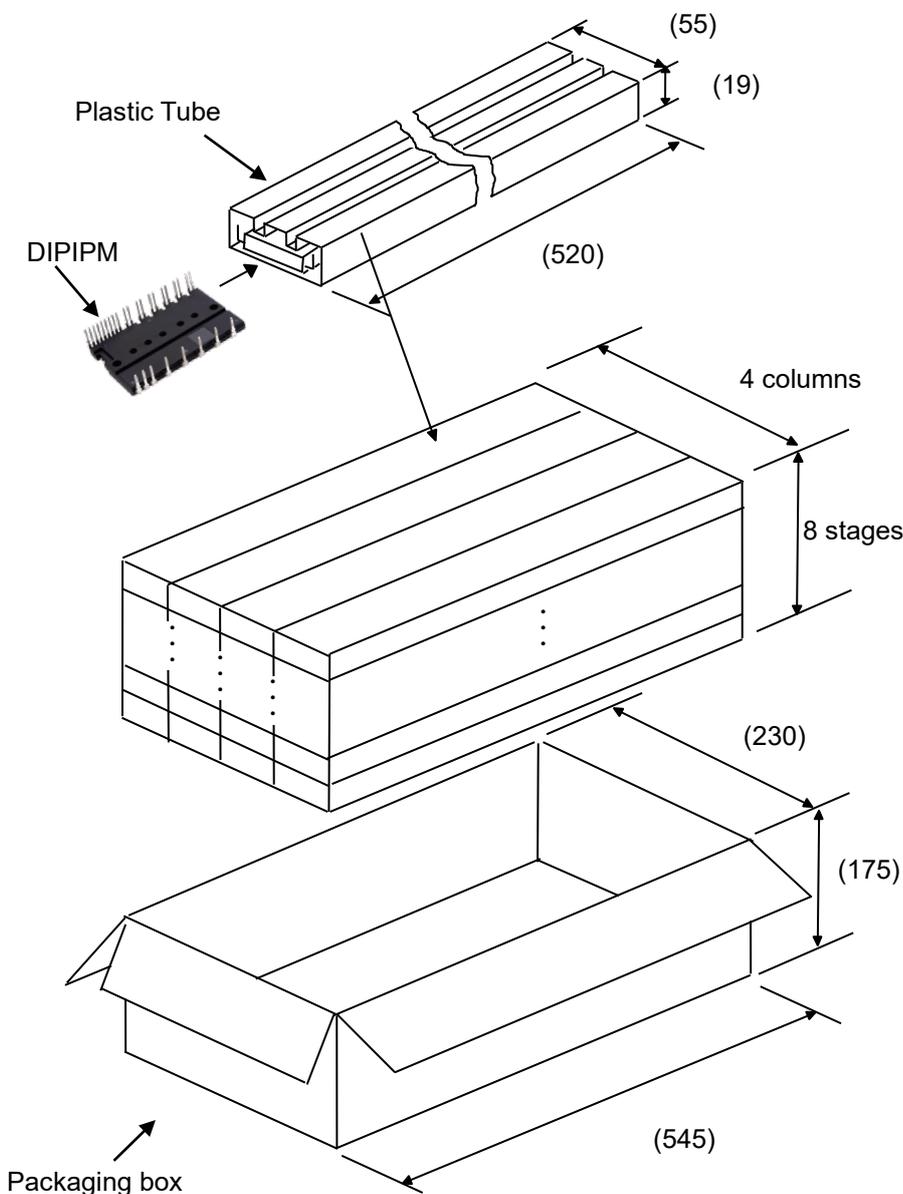
Fig.4-4-2 Example of waveform by one charging pulse

Initial charging needs to be performed until voltage of BSC exceeds recommended minimum supply voltage 13V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for reset of internal IC state before starting system. Input pulse width is needed to be longer than allowable minimum input pulse width $PWIN(on)$. (e.g. $0.7\mu s$ or more for PSSxxS71F6 and $1.0\mu s$ or more for PSSxxS51F6. Refer the datasheet for each product.)

CHAPTER 5 PACKAGE HANDLING

5.1 Packaging Specification



Quantity:

- 9pcs per 1 tube (PSSxxS71F6)
- 10pcs per 1 tube (PSSxxS51F6)

Total amount in one box (max):

- Tube Quantity: 4 × 8=32pcs
- IPM Quantity(max.):
- 32 × 9=288pcs (PSSxxS71F6)
- 32 × 10=320pcs(PSSxxS51F6)

When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the space of top stage.

Weight (max):

- PSSxxS71F6
- About 21g per 1pcs of DIIPM
- About 300g per 1 tube
- About 11kg per 1 box
- PSSxxS51F6
- About 20g per 1pcs of DIIPM
- About 310g per 1 tube
- About 12kg per 1 box

Spacers are put on the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.5-1 Packaging Specification

5.2 Handling Precautions

 <h1 style="font-size: 2em; margin: 0;">Cautions</h1>	
Transportation	<ul style="list-style-type: none"> ·Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ·Throwing or dropping the packaging boxes might cause the devices to be damaged. ·Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	<ul style="list-style-type: none"> ·We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	<ul style="list-style-type: none"> ·When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	<ul style="list-style-type: none"> ·Keep modules away from places where water (including dew condensation) or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	<ul style="list-style-type: none"> ·The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable.
Static electricity	<ul style="list-style-type: none"> ·ICs and power chips with MOS gate structure are used for the DIIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. <p>(1)Precautions against the device destruction caused by the ESD The ESD of human bodies and packaging and/or excessive voltage applied across the gate to emitter may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity.</p> <ul style="list-style-type: none"> ·Containers that charge static electricity easily should not be used for transit and for storage. ·Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. ·Should not be taking out DIIPM from tubes until just before using DIIPM and never touch terminals with bare hands. ·During assembly and after taking out DIIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. ·When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. ·If using a soldering iron, earth its tip. <p>(2)Notice when the control terminals are open</p> <ul style="list-style-type: none"> ·When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction. ·Short the terminals before taking a module off.

Important Notice

The information contained in this datasheet shall in no event be regarded as a guarantee of conditions or characteristics. This product has to be used within its specified maximum ratings, and is subject to customer's compliance with any applicable legal requirement, norms and standards.

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