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Transition to SiC MOSFETs while maintaining the established NX Package Outline

The transition to power modules based on SiC MOSFET technology from Si IGBT technology is inevitable. However, form factor preferences which are carry-overs from the Si IGBT era still impede the commercialization of SiC technology as they have been known to have high parasitic inductance. Mitsubishi Electric has broken this deadlock by developing a modified NX package with an internal busbar structure suitable for SiC MOSFETS.

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Introduction:
The Si IGBT chip technology has evolved over the past decades and the improvements gained from one chip generation to the next keep getting narrower (refer Figure 1). This indicates that each new generation is coming closer to the physical limits of the material itself.

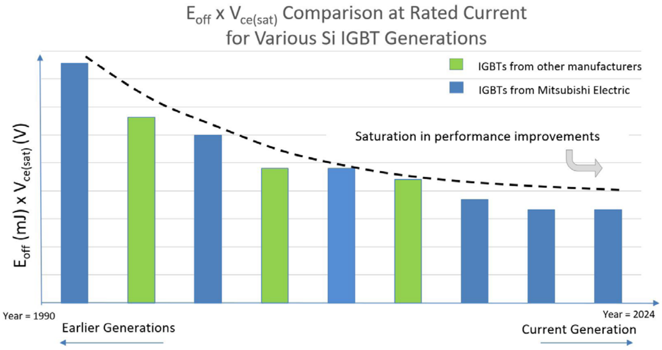

Figure 1: E_{off} versus $V_{CE(sat)}$ Comparison for various Si IGBT Generations

Wide band gap semiconductors such as SiC MOSFETs offer the possibility of achieving a significant reduction in the overall semiconductor power losses. One aspect of the potential loss reduction using SiC MOSFETs comes from the possibility to reduce switching losses allowing an increase in the switching frequency. As a result, the filter components can be optimized and the corresponding losses would come down leading to an overall reduction in the system losses.

The challenge: Packaging consideration for SiC MOSFETs:
Switching loss reduction with SiC MOSFETs is possible because they can be switched much faster than Si IGBTs. However, there are certain challenges in realizing high switching speeds during operation of the power module.

Switching overvoltage: The inductive voltage overshoot during turn-off of the MOSFET (ΔV_{DS}) is a function of the stray inductance (L_S) of the power module package and the rate of change of drain current ($\frac{dI_D}{dt}$).

$$\Delta V_{DS} = -L_S \; x \; \frac{dI_D}{dt}$$

It can be inferred from Figure 2 that higher the internal inductance of the package is, lower is the maximum allowable $\frac{dI_D}{dt}$.

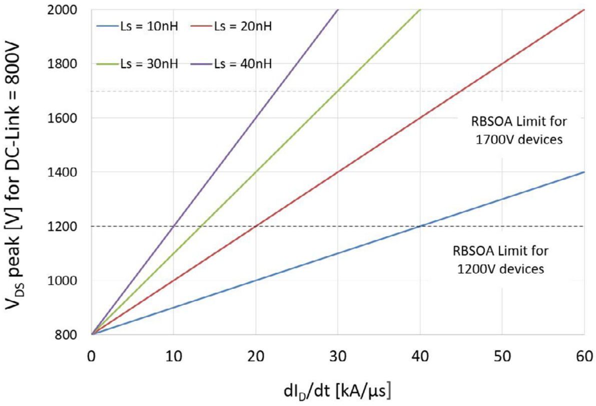

Figure 2: V_{DS} peak versus $\frac{dI_D}{dt}$.

Internal current balancing: The current rating of a power module depends up on the number of individual dies which can be connected in parallel inside the package. It is important to maintain a homogenous distribution of drain current between the chips during both static and dynamic operation. Therefore, the power module package has to be designed to ensure proper current balancing of the individual dies.

Formfactor preference and challenges: Half bridge Si IGBT modules belonging to 650V, 1200V or 1700V classes having a rated current in the range of several hundred amperes are widely available in the NX package which has established itself in the industrial power conversion segment since several years. Ideally, it would be advantageous to maintain the existing power module form factor (such as the established NX package). However, the conventional NX package has an internal inductance (L_S) in the range of about 20 nH making it unsuitable for SiC adoption. In addition, as evident from the representation in Figure 3, conventional NX package requires that the Si IGBT dies be placed along the long axis of the power module. As a result, the dynamic current sharing between the dies are is not optimal and therefore present a challenge for direct SiC adoption.

The solution: low inductance NX package for SiC adoption:
The internal layout of the NX package has been modified for SiC adoption. The internal cross section of the modified NX package is shown in Figure 4.

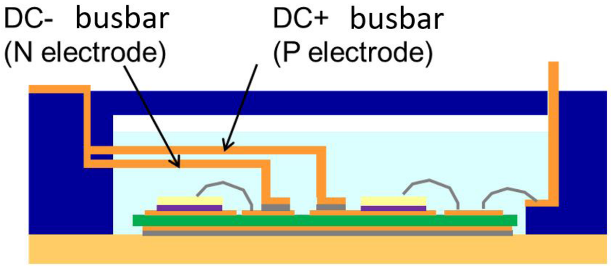

Figure 4: Internal cross section of the modified NX package for SiC adoption

The DC+ and DC- busbars are arranged in a 'laminated structure' placed as close to each other as possible (separated by an insulation layer) for maximizing magnetic field compensation. In addition, the DC+ and DC- busbars are directly bonded to the substrate avoiding additional stray inductance by bond wires connections to the terminals. Furthermore, the dies are not placed along the long axis of the module (as was the case with the conventional NX design using Si IGBTs). An optimized circuit pattern has been developed (refer Figure 5) in order to achieve optimum current sharing between the different dies. The internal inductance of the modified low inductance NX module has been measured to be 9nH. This is around 47% reduction of parasitic inductance in comparison with the conventional NX power module.

Product description:
The NX SiC module has been released in the 1700V/600A rating (FMF600DXE-34BN) and 1200V/600A rating (FMF600DXE-24BN). Both devices have the half bridge topology (2in1 configuration). The power module consists of an ceramic baseplate (AlN substrate) and utilizes silicon gel encapsulation. The power modules are based on Mitsubishi's 2nd generation SiC chip technology.

Performance benchmarking:
In order to understand the performance improvement using the modified SiC NX module, a benchmarking can be carried out considering the following items:

I. Impact of the modified NX package (versus the conventional NX package)
II. Performance benchmarking of the SiC MOSFET chip technology itself (versus Si IGBT technology)

Item I can be analyzed using the trade-off relationship shown in Figure 7 - the inductive voltage overshoot (V_{DS} $[V]$ for SiC MOSFETs and V_{CE} $[V]$ for IGBTs) and the turn-off switching energy (E_{off} [mJ/Pulse]). The following inferences can be obtained from Fig. 7: considering the operation conditions DC-Link = 1000V, I_C (or I_D) = 600A and T_{vj} = 150°C

a) Conventional NX package: The red curve indicates the V_{CE} $[V]$ for the 7th generation 1700V Si IGBT and the for the 1700V 2nd gen SiC MOSFET considering the conventional NX package ($L_S = \sim 20nH$). It is possible to achieve lower turn-off losses (E_{off}) using the SiC MOSFET in the same (conventional) package, however the inductive voltage overshoot cannot be maintained within the RBSOA (Reverse Bias Safe Operating Area) with an adequate safety margin.
b) Modified low inductance NX package: The blue curve indicates the V_{DS} for the 1700V SiC MOSFET considering the modified low inductance NX package. It can be seen that the RBSOA can be maintained in a safe limit without compromising the E_{off}. Since the $L_S = 9nH$, a lower turn-off gate resistance can be selected.

Item II can be analyzed using Figure 8 which presents the power loss and junction temperature comparison of the 7th gen 1700V Si IGBT (in the conventional NX package) and the 2nd gen SiC MOSFET (in both the conventional and the low inductance NX package). The conclusion from Figure 8 is: about 72% reduction in power losses versus the Si IGBT module is possible by adopting the modified low inductance SiC MOSFET while maintaining the NX package outline. As a result, the switching frequency can be increased by a factor of 5 (enabling significant filter optimization) while keeping the maximum junction temperature below the maximum specified value.

Figure 6: A photo of the NX SiC module

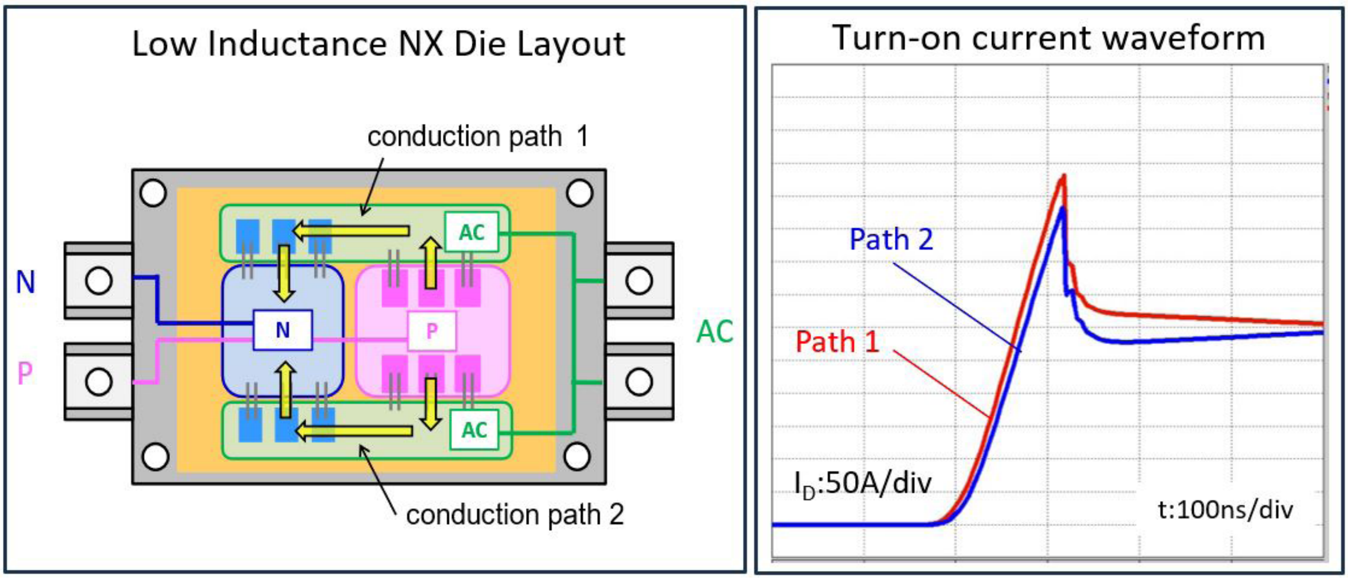

Figure 5: Internal layout of the modified NX package (left), turn-on current waveform for the modified NX package (right)

Conclusions:

In order to maintain the competitive edge and also to be economical for the end-user, a certain level of efficiency and compactness becomes advantageous for every power conversion application. Each generation of Si IGBT has successfully displaced its previous generation with the same argument – better power loss performance. As developments in Si IGBT technology reach saturation, SiC MOSFETs become more and more attractive. The last technical frontier for full transition to SiC from Si is – the form factor for power modules with Si IGBTs. The modified low inductance NX package along with the 2nd generation SiC MOSFETs from Mitsubishi Electric aims to solve this riddle and thereby offer a viable solution for a variety of power conversions.

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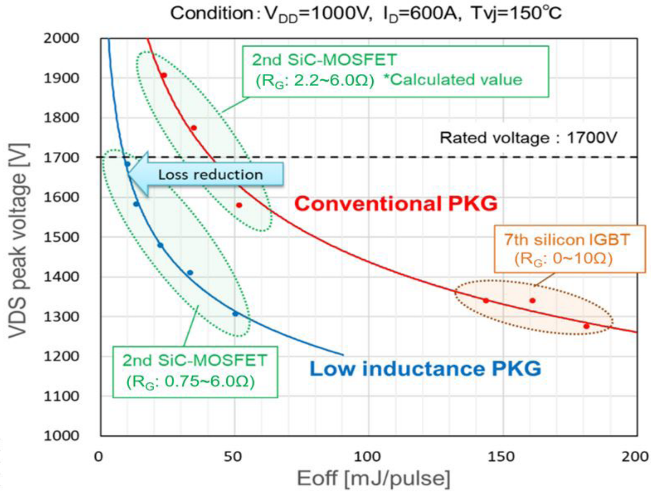
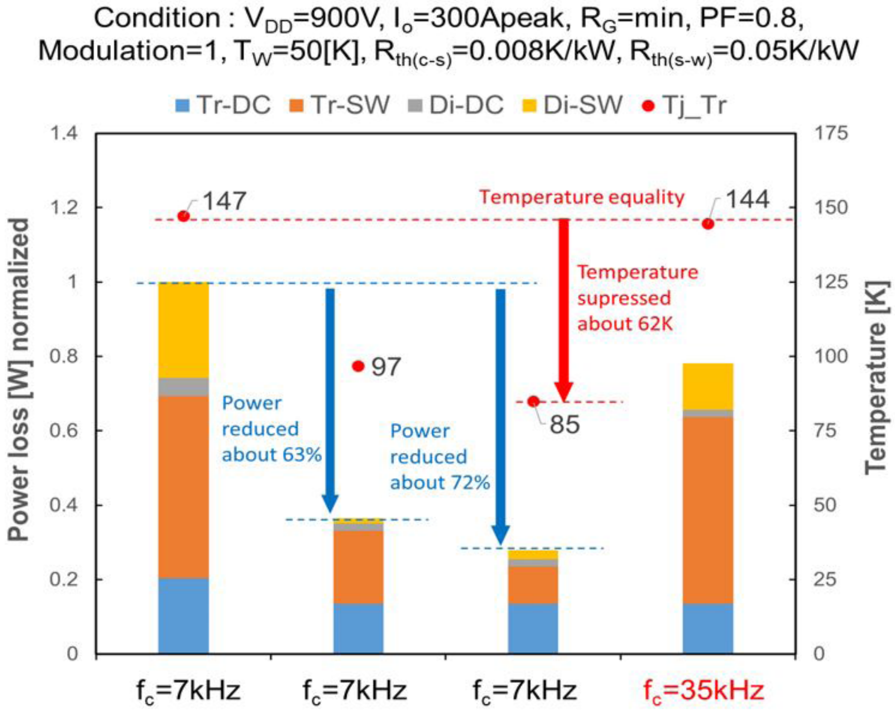


Figure 7: V_{DS} peak versus E_{off} for 2nd gen SiC considering the conventional NX package and the new low inductance NX package. 7th gen Si IGBT performance is included for reference.



chip	7th Si-IGBT	2nd SiC-MOSFET	
package	Conventional NX		Low inductance NX

Figure 8: Normalized power loss for 7th gen Si IGBT and 2nd gen SiC considering the conventional and the new low inductance NX package