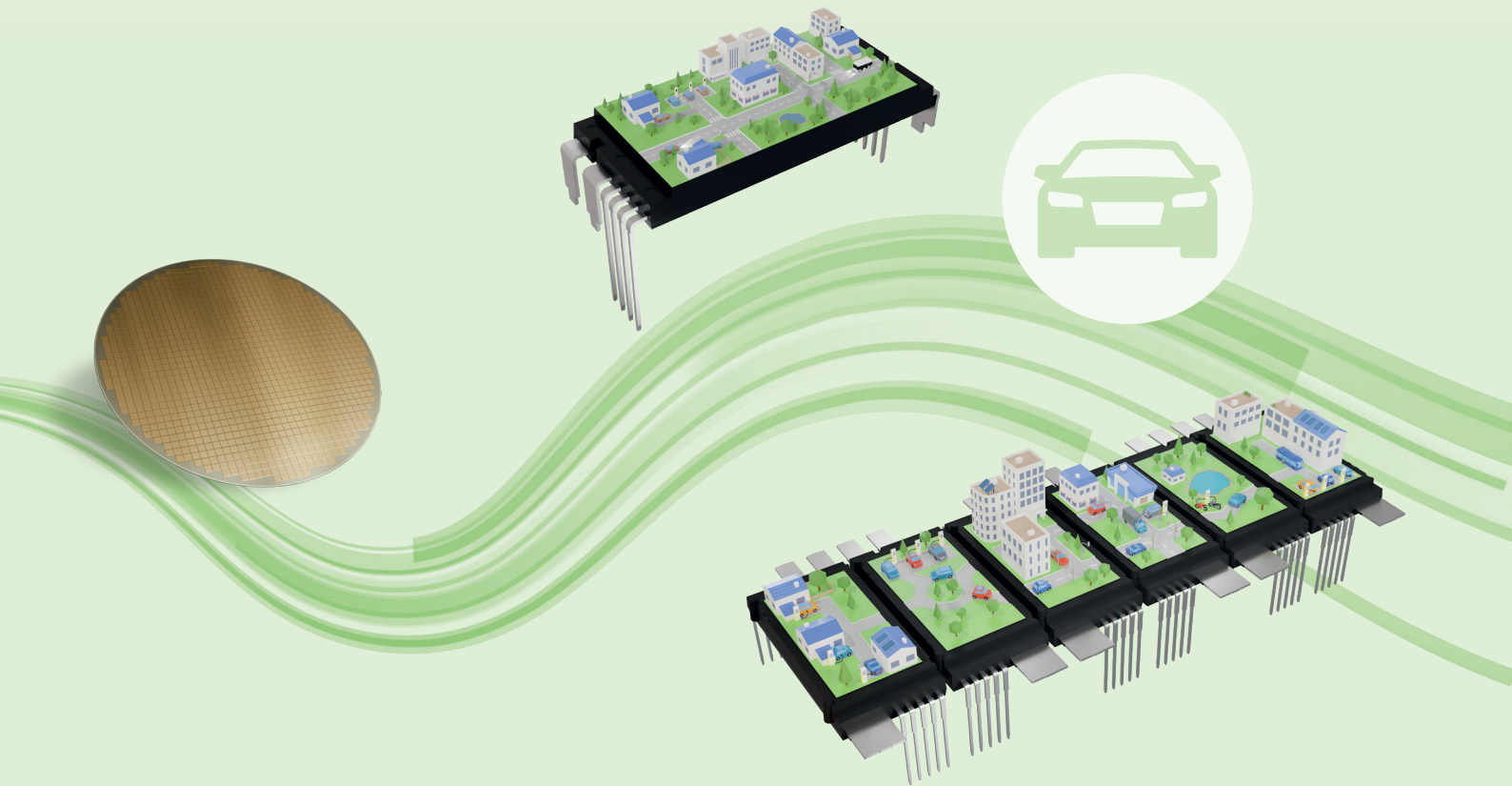
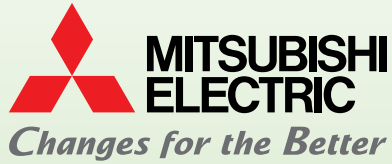


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Electronics in Motion and Conversion

September 2025



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Bare-Dies and Scalable T-PM for E-Mobility:
Advanced SiC MOSFET & Si RC-IGBT Devices

Next-Gen SiC MOSFET & Si RC-IGBT: Bare-Dies and Transfer Mold Power Modules

High-Power-Density, High-Efficiency & Scalability for E-Mobility

With accumulated track record of over 34 million xEVs driven by its highly reliable power devices since 1997, Mitsubishi Electric is steadily moving forward in advancing its next generation of finely coordinated, in-house designed & developed efficient semiconductor bare-dies (SiC MOSFET & Si RC-IGBT) and compact high-reliability transfer mold packaging (T-PM) technologies meeting the ongoing trend towards high power-density, scalable, cost-effective reliable solutions for e-Mobility.

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Introduction

As the world faces the escalating crisis of climate change, the automotive industry is increasingly undergoing a transformative shift towards power train electrification. Electrified vehicles (xEVs), including hybrid and fully electric powertrains, are at the forefront of this transition, demanding innovative solutions that balance performance, reliability, cost, and efficiency.

To meet these evolving requirements, power electronic devices in xEVs must address several critical challenges: delivering high power and efficiency, withstanding harsh automotive environments, maintaining cost-effectiveness, and supporting intelligent integration. Power semiconductor devices are central to achieving these objectives. In particular, two technologies have emerged as key enablers: Silicon Carbide (SiC) MOSFETs and Reverse Conducting Si IGBTs (RC-IGBTs). Each offers distinct advantages tailored to specific application needs. SiC MOSFETs are ideal for high-power, high-frequency applications such as traction inverters, where efficiency, thermal performance, and power density are paramount. RC-IGBTs provide a cost-effective alternative by integrating both the IGBT and freewheeling diode in a one die design, making them suitable for applications where cost and moderate performance demands must be balanced.

General Outline of Automotive Products

Recognizing the diverse requirements of 400V and 800V xEV architectures, Mitsubishi Electric offers a robust portfolio of both bare die power devices and scalable power modules, including both SiC MOSFETs and Si RC-IGBTs technologies. These technologies represent the company's ongoing commitment to innovations that are linked to addressing the real-world challenges of next-generation electric vehicles.

Key factor in Mitsubishi Electric's automotive power devices success lies in the fine coordination of in-house designed and developed efficient semiconductor devices (SiC & Si) and compact high-reliability transfer mold packaging (T-PM) with Direct-Lead-Bonding (DLB) technology eliminating the wire-bonding limitation usually faced in conventional packages.

Overview of Mitsubishi Electric automotive bare-die products lineup is given in Figure1(a) for SiC MOSFET and RC-IGBT. Both technologies contain devices with blocking voltage ratings of 750V and 1200V/1300V. Gen 4 SiC and 3rd Gen. RC-IGBT bare dies are integrated inside the latest automotive power modules family: the J3-Series, shown in Figure1(b) [1].

The core-module, J3-T-PM, is a compact half-bridge that can be fitted with either SiC MOSFET or Si RC-IGBT, enabling solutions for both 800V and 400V battery classes within the same module footprint along with various built-in features. The J3-T-PM is solderable, in a modular way (J3-HEXA-S/L), to pinfin baseplate or directly to the cooling-structure of the inverter, covering a wide power range from 80kW to over 300kW~.

The following two parts of this article will explore the technical foundations and advantages of Mitsubishi Electric's SiC MOSFET and Si RC-IGBT device technologies, illustrating how they contribute to advancing xEV powertrain performance and supporting successful adoption.

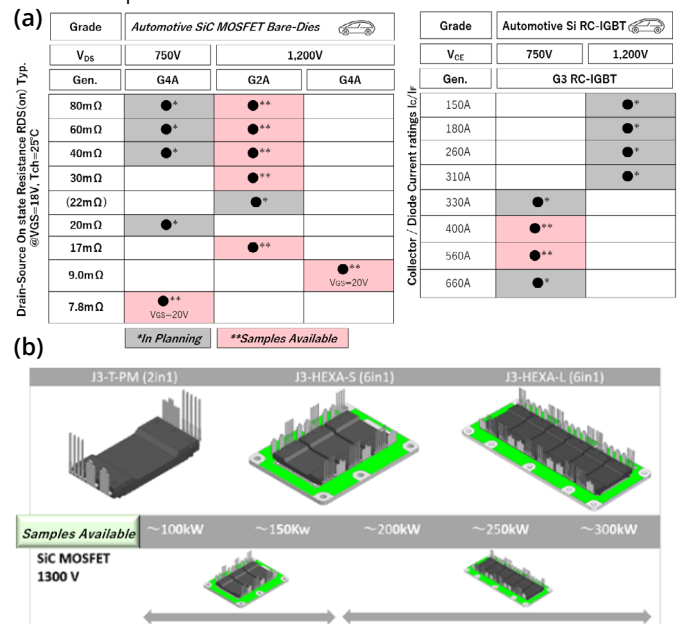


Figure 1: Lineup (a) SiC MOSFET and RC-IGBT bare dies (b) J3-series SiC/RC-IGBT power modules packages

Part-1

Evolution of Mitsubishi Electric's SiC MOSFET

Since the 1990s, Mitsubishi Electric has gained comprehensive experience in the design, development, and production of SiC devices for various high-efficiency demanding applications ranging from home air-conditioners to railway traction drives.



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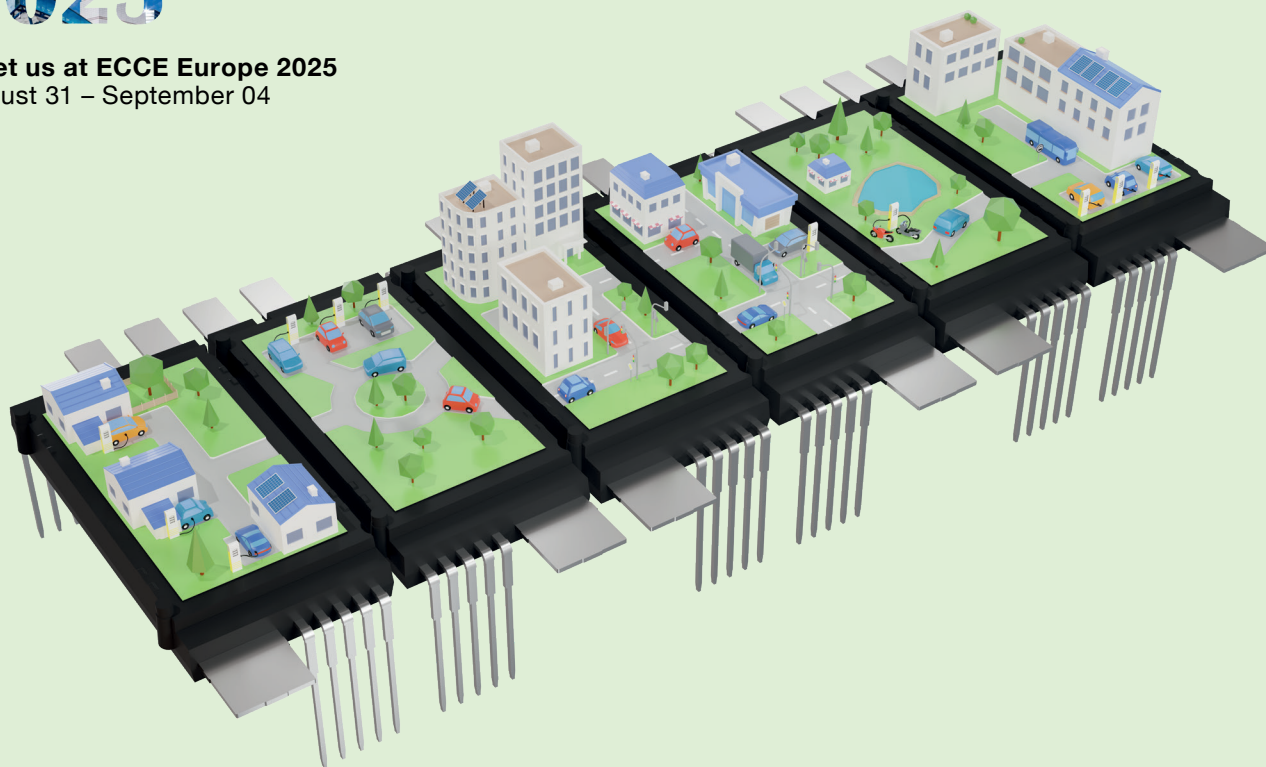
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- // In-house developed, high-efficiency Si RC-IGBT and SiC MOSFET bare dies enable superior performance
- // Compact, high-reliability transfer mold packaging (T-PM) with optimized matching bare dies, ensuring enhanced thermal performance, scalability, and long-term durability
- // Half-bridge core module (J3-T-PM) compatible with 1300 V SiC MOSFETs and 750 V Si RC-IGBTs
- // Modular design approach (J3-HEXA-S/L) by soldering J3-T-PM to a pin-fin baseplate or directly to the inverter's cooling structure
- // Enabling scalable power level design concepts, from 80 kW to over 300 kW, to meet the growing demand for high power-density

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As shown in Figure 2, several generations have been introduced, featuring optimized cell sizes, improved carrier doping profiles and gate structures. Currently, Mitsubishi is steadily advancing forward developing next generations of innovative Planar SiC-MOSFETs as well as Gen.4~ Gen.5 with Trench structures. In parallel with the existing 6-inch facility, the full introduction of a new advanced 8-inch SiC wafer processing plant is scheduled for 2026 [2, 3]

Due to their various attractive features that meet e-Mobility requirements, Trench SiC MOSFET devices are of particular focus.

The following subsections will highlight some of the key innovative design concepts and technologies that have contributed to Mitsubishi Electric's success in optimizing the challenging trade-offs of trench-structures. Further, promising recent study results on the influence of proton implantation on SiC MOSFET electrical characteristics and bipolar degradation suppression will be discussed.

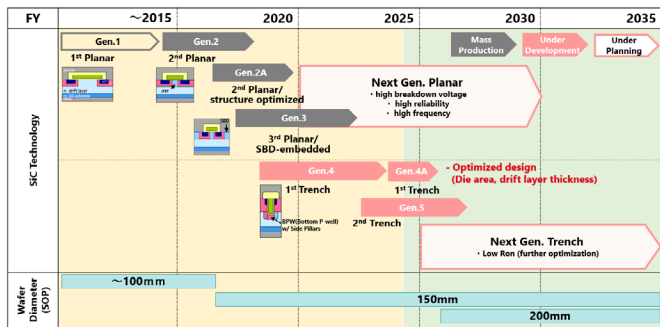


Figure 2: SiC MOSFET Roadmap

Optimizing R_{dson} vs Short-Circuit-Capability vs Switching-Loss Trade-off

One of the key advantages of Trench gate SiC MOSFET is that it realizes low on-resistance (low DC-losses/high-efficiency) because of its improved channel structure and high MOS channel density. However, high conductivity means it is extremely difficult to ensure short-circuit capability if a short-circuit occurs in the device. Hence, incorporating additional methods for controlling short-circuit capability in the device structure design is essential. Another important trade-off aspect to consider is the classical DC-loss vs Switching-loss where optimization is also essential. To address these important trade-offs, Mitsubishi Electric has developed proprietary trench-type SiC-MOSFETs with a unique structure that enables lower resistance, higher reliability and lower switching losses [4, 5]. The schematic of the developed trench SiC-MOSFET structure is shown in Figure 3 and its key features are realized by three unique implanted layers briefly summarized in the following:

- (1) P-type protective layer (BPW: Bottom P-Well) for relaxing the electric field applied to the bottom of the trench,
- (2) Sidewall P-type pillar (SP: Sidewall Pillar) for grounding the BPW, and
- (3) N-type Junction Field Effect Transistor (JFET) doping layer (JD: JFET Doping) for preventing narrowing of the current path.

Highlighting the unique feature of this structure, by adjusting the area density SP ratio (r_{SP}), defined as SP area/sidewall area, trade-off control between on-resistance and short-circuit capability could be realized as shown in Figure 4 (a-c). For example, designing r_{SP} as 2, a favorable performance of short circuit withstanding time (t_{SC}) of 2.2 μs with $R_{\text{on,sp}}$ as low as 2.2 $\text{m}\Omega\text{cm}^2$ @RT and 3.9 $\text{m}\Omega\text{cm}^2$ @150°C could be achieved.

Further, switching evaluation results confirmed that higher r_{SP} leads to lower loss at turn-off (E_{off}) and higher loss at turn-on (E_{on}). To compare with regards to the total DC and AC losses, calculations based on $R_{\text{on,sp}}$ @150°C; E_{on} and E_{off} @ $R_{\text{g}}=5 \Omega$ at the assumption of 20 kHz switching frequency with 49% duty cycle were performed. As shown in Figure 4(d), r_{SP} optimization brings improved t_{SC} without increase in AC loss but at the penalty of a slight increase

in DC loss. Hence, because of the developed structure, the trade-off relationships between DC/AC losses and t_{SC} can be adjusted by designing r_{SP} in accordance with the specific application requirements. This flexible performance controllability represents a clear improvement over conventional trench SiC-MOSFET structures.

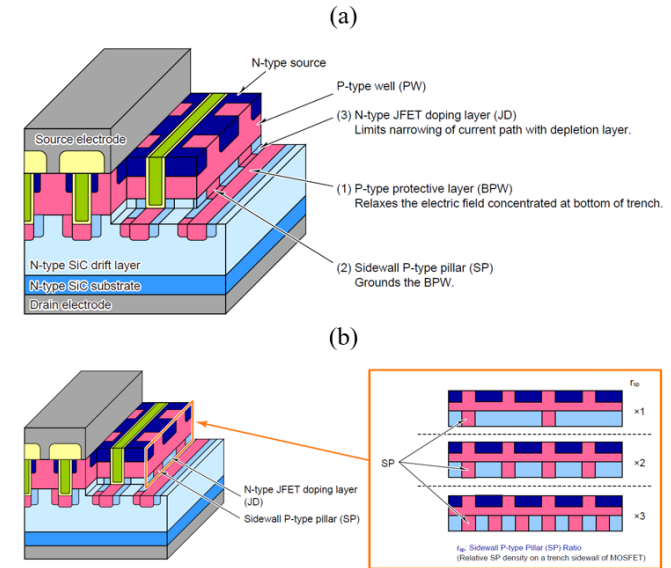


Figure 3: (a) Schematic of Mitsubishi proprietary trench SiC-MOSFET structure and (b) its controllable Sidewall P-type Pillar (SP) Ratio r_{SP}

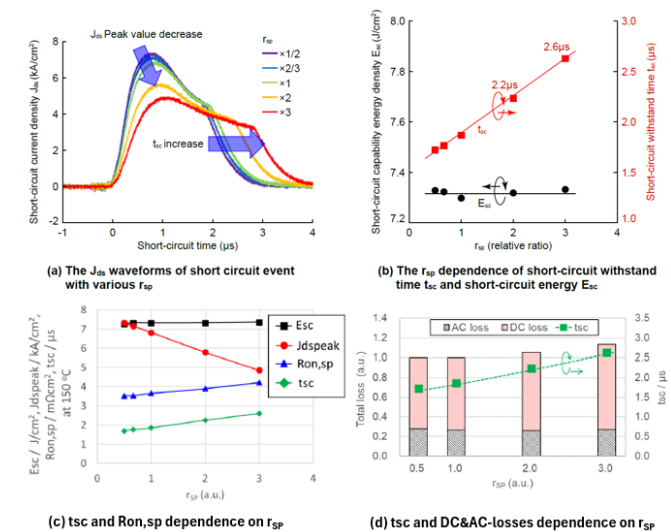


Figure 4: (a) waveforms of short circuit event with various r_{SP} (b) short-circuit withstand time t_{SC} and short-circuit energy E_{sc} dependence on r_{SP} , (c) t_{SC} and $R_{\text{on,sp}}$ dependence on r_{SP} , (d) t_{SC} and DC&AC-losses dependence on r_{SP}

Realizing proton implantation positive influence on SiC MOSFET electrical characteristics and bipolar degradation suppression

Rather than adding an externally paralleled Schottky barrier diode (SBD), utilization of the body-diode of SiC MOSFET devices represents a very important aspect to realize compact and cost-effective power device solutions. However, bipolar degradation is a key issue that must be addressed when utilizing the bipolar operation in SiC power devices. Suppression of bipolar degradation with proton implantation technique has been reported as a possible approach. However, proton implantation is a complex process that can have both positive and negative effects on the electrical characteristics of 4H-SiC MOSFETs. Understanding these effects is crucial for designing and optimizing SiC power devices, particularly for automotive applications [6]. Following an optimized proton implantation approach, Mitsubishi Electric fabricated and evaluated, on experimental bases, very large numbers of proton implanted 4H-SiC

MOSFETs (about 4,000 chips) to verify statistically its effectiveness in the suppression of the bipolar degradation as well as to consider its technological applicability to mass production process.

The cross-sectional schematics and flowchart of the evaluated SiC MOSFETs with and without proton implanted layer is shown in Figure 5 (a) and (b) respectively. The applied proton doses are $1 \times 10^{12}/\text{cm}^2$, $1 \times 10^{13}/\text{cm}^2$ and $1 \times 10^{14}/\text{cm}^2$.

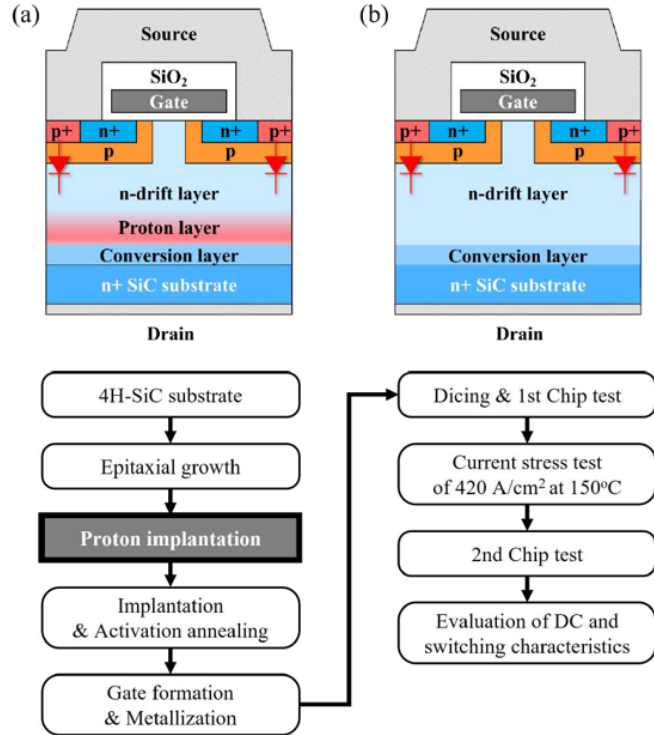


Figure 5: Schematics and flow chart of evaluated SiC MOSFETs (a) with proton implanted layer and (b) without proton implanted layer

After passing the initial 1st chip test, the fabricated devices were stressed by applying continuous current (typically, $V_{GS}=0$ V, $t=2$ min, $T=150^\circ\text{C}$ and $J_{SD}=420$ A/cm²) to the body diodes to evaluate the bipolar degradation suppression level. The reference for a “degraded” device was defined as an on-resistance increase of over 3% after the current stress. The numbers of the tested samples were 1270 (w/o), 880 ($1 \times 10^{12}/\text{cm}^2$), 844 ($1 \times 10^{13}/\text{cm}^2$) and 823 ($1 \times 10^{14}/\text{cm}^2$).

A summary of the DC-characteristics evaluation results after the current stress can be explained with the help of Figure 6 in the following:

- The positive impact of the proton implantation on the suppression of the SiC MOSFET bipolar degradation is clearly evident from these experimental results.
- With a proton dose of $1 \times 10^{14}/\text{cm}^2$, degraded MOSFET ratio significantly drops to about 3%, which is roughly 1/4th the value without proton implantation.
- The forward DC-characteristics were not influenced, and the only noticeable change was in the 3rd-quadrant (I_{SD} -vs- V_{SD} @body-diode mode) with an increase in the differential on-resistance (Figure 6(a) & (b)) and clear suppression of temperature dependence @ a proton dose of $1 \times 10^{14}/\text{cm}^2$ (Figure 6 (c)).
- With the body diode conducting only during the dead time under normal pulse width modulation (PWM), this 3rd-quadrant change is considered insignificant because it hardly affects the total loss.
- On the contrary, the suppression of temperature dependence in the 3rd-quadrant can be considered another positive impact of the proton implant because it helps eliminating current-imbalance among paralleled chips. In other words, this helps to evenly distribute dead-time current-stress among paralleled body-diodes instead of being focused on the hottest chip.

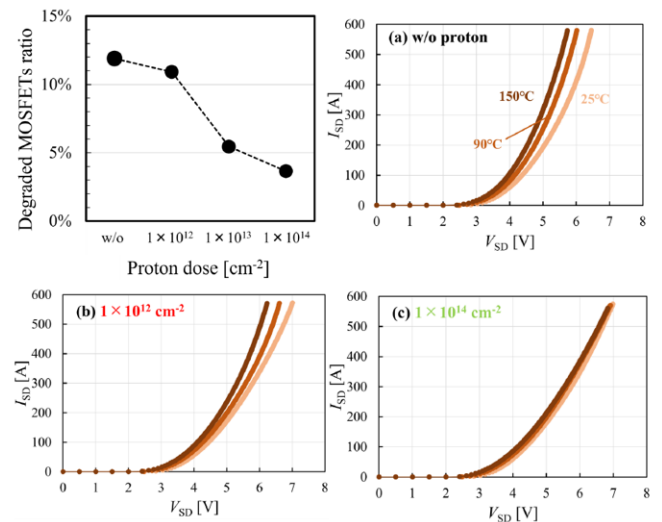


Figure 6: The ratio of the degraded MOSFETs after current stress in each proton dose condition and the influence on the body-diode 3rd-quadrant ($V_{GS}=-10$ V).

Finally, the impact of the proton implant on the switching characteristics of the body diode of current-stressed samples was evaluated under the conditions: Double pulse testing @ $V_{DS}=760$ V; $I_{DS}=380$ A; $V_{GS(lower)}=-5$ V; $V_{GS(upper)}=-5/+22$ V; 150°C .

A summary of the switching-characteristics evaluation results after the current-stress can be explained with the help of Figure 7 in the following:

- The positive impact of the proton implantation on the suppression of the SiC MOSFET reverse-recovery oscillations as well as surge-voltage is clearly evident from these experimental results.
- With a proton dose of $1 \times 10^{14}/\text{cm}^2$, SiC MOSFET body diode waveforms show favorable recovery characteristics enabling faster switching speeds for higher efficiency with less EMI noise concerns
- Significant Q_{rr} and ΔV reduction (58% and 96% respectively in this example) enabling higher efficiency and safe SiC MOSFET operation

Given the achieved promising results summarized above, establishing a suitable proton implantation condition will surely open the way for its introduction to the future mass production of bipolar-tolerant and reliable SiC MOSFETs. Further comprehensive optimization investigations are ongoing considering performance and other factors.

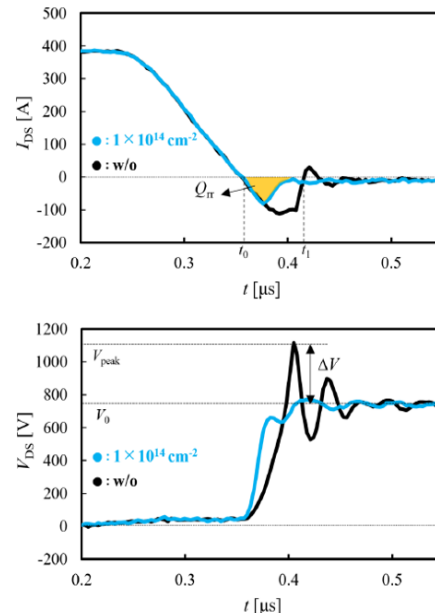


Figure 7: Reverse recovery waveforms of the body diode of current-stressed samples with & w/o proton implantation

At the end of Part-1 of this article, a brief representative example of the performance capability of Mitsubishi Gen.4 Trench SiC-MOSFET chips when installed on the scalable J3-Series automotive modules is given in Figure 8. The example is based on inverter output RMS current vs switching frequency at an operating temperature of 175°C, with a main battery voltage of 800V, coolant temperature of 65°C, and coolant flow rate of 10 l/min.

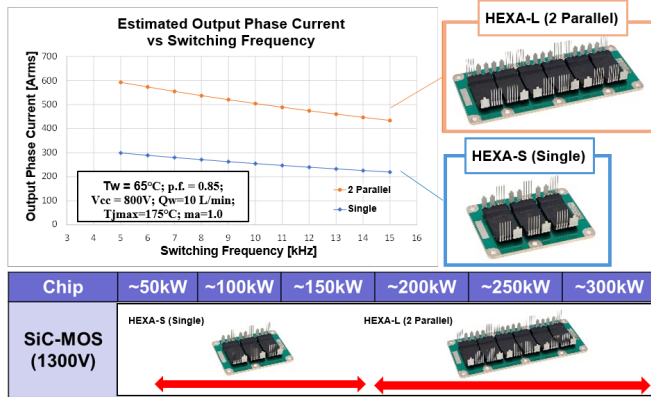


Figure 8: Representative example of the performance capability of Gen.4 Trench SiC-MOSFET chips on the scalable J3-Series automotive modules

Part-2

Evolution of Mitsubishi Electric's RC-IGBT

The Reverse-Conducting Insulated Gate Bipolar Transistor (RC-IGBT) is an advanced power semiconductor device developed and continuously refined by Mitsubishi Electric. Designed to enhance efficiency, reduce system size, and lower overall costs, the RC-IGBT integrates both the IGBT and the freewheeling diode into a single chip which eliminates the need for an external diode, as required in traditional IGBT-based systems. This integration not only simplifies circuit design but also reduces component count and wiring between dies.

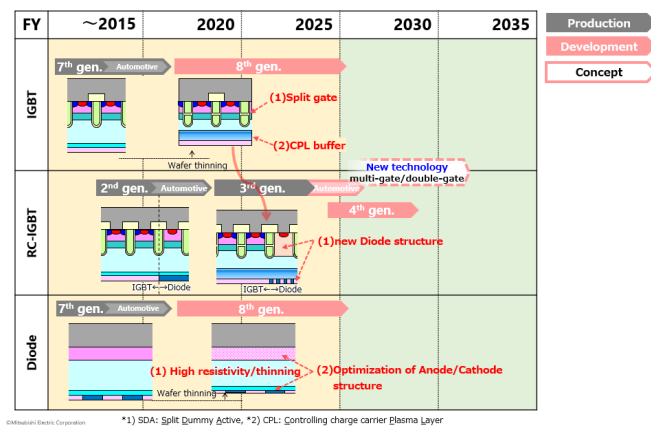


Figure 9: Transition of RC-IGBT Development

Figure 9 illustrates the evolution of RC-IGBT development at Mitsubishi Electric. In 2006, the company launched the world's first-generation RC-IGBT, marking its initial application in motor control power modules for white goods [8, 10]. Building on this success, Mitsubishi Electric introduced the second-generation RC-IGBT in 2015 [9]. This version based on latest development of Carrier-Stored-Trench-Gate-Bipolar-Transistor (CSTBT™) at that time (7th Gen IGBT) structure optimized through microfabrication and thin-wafer technology, significantly reduced conduction and switching losses. Initially used in industrial applications, it was later adopted for automotive applications due to its superior performance. Currently, Mitsubishi Electric is developing the third-generation RC-IGBT based on 8th generation of CSTBT™ and diode. The advanced technologies and design improvements that is implemented in this generation will be highlighted in the following sections.

Advantages of Single-Chip RC-IGBT

This single-chip solution integrating both IGBT and free-wheeling diode offers several advantages over conventional discrete-component designs in terms of thermal performance, electrical efficiency, and mechanical integration.

1. Optimized Chip Utilization and Module Miniaturization

The shared structures such as the guard ring can be utilized. This not only reduces the total chip area required but also eliminates redundant or unused spaces between separate components. As a result, module size can be significantly reduced, contributing to more compact system designs.

2. Improved Heat Dissipation Through Chip Integration

In motor control applications, the diode can generate a large amount of heat in a short time, especially under fault conditions such as a motor lock. This instantaneous heat generation poses a challenge for thermal design and can restrict the allowable current through the system.

RC-IGBT addresses this condition by physically integrating the IGBT and diode into the same silicon die. This integration leads to:

- Expansion of the heat dissipation path: Thermal energy can spread more evenly across the larger, unified chip area, refer to Figure 10 (a).
- Reduction of thermal resistance: A single heat flow path reduces the temperature rise during high-load operation.

Due to staggered heat generation between the IGBT and the diode, they do not produce peak heat simultaneously. This temporal separation reduces thermal stress, improving the overall reliability and current-carrying capability of the device.

Electrical Performance Gains Through Simplified Internal Wiring

In traditional module layouts with separate chips, longer internal wiring is required for interconnection. The resulting high parasitic inductance can degrade switching performance and increase EMI. By integrating the components into a single chip, internal wiring can be significantly shortened (refer to Figure 10 (b)), reducing inductance and associated voltage spikes during switching which leads to:

- Greater design flexibility: Internal layouts can be optimized to suit various thermal or electrical requirements.
- Better use of space: The saved space can be used to incorporate larger chips for increased current capacity, or to shrink the module further, supporting miniaturization of the final product.

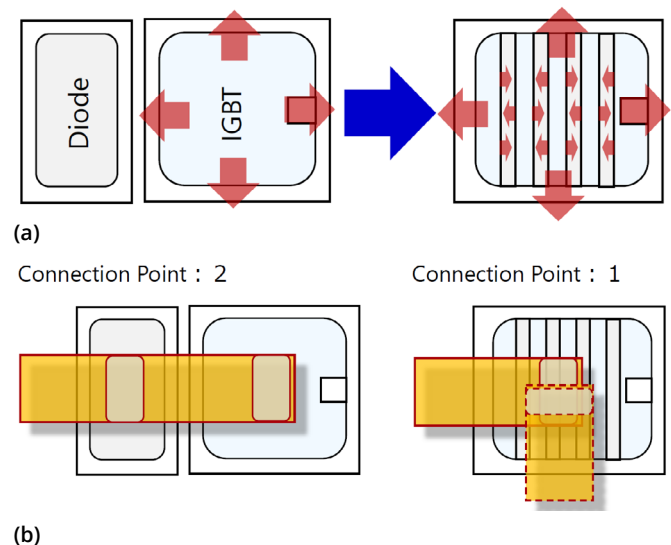


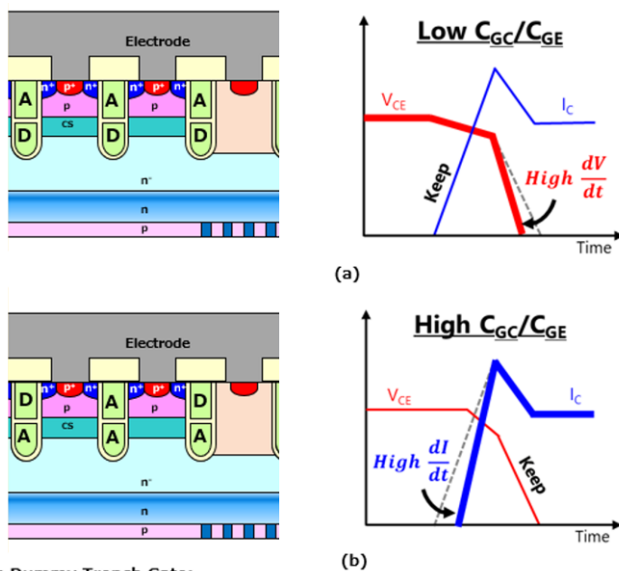
Figure 10: Benefits of integrating IGBT and FWD into one Chip (a) improved heat dissipation (b) simplifying internal wiring

3rd Generation Reverse Conducting IGBT

The design of RC-IGBT requires not only the technology to reduce power loss by optimizing the structure inside the IGBT and thinning the wafer, which are common issues with single IGBTs, but also the technology to improve heat dissipation through the free-diode structure design and layout design inside the chip, which are unique to RC-IGBTs. The following four technologies are considered in the design optimization or 3rd Gen RC-IGBT to meet both reliability, power losses and thermal design requirements [10].

a) Optimization Technology for Gate Capacitance of MOS Structure

To reduce switching loss, recent advancements focus on optimizing gate capacitance. Conventional gate control adjusts the gate resistance (R_g), but this simultaneously affects both di/dt and dV/dt , limiting optimization. To overcome this, the 3rd Gen RC-IGBT introduces a two-stage trench gate structure as shown in Figure 10, enabling independent control of CGE and CGC. This expands the tunable range of the CGC/CGE ratio, allowing targeted improvement of either di/dt or dV/dt without compromise. For example, with Split gate technology (Figure 11 (a)) lowering CGC/CGE increases dV/dt , reducing turn-on loss (E_{on}) by 20%, while increasing CGC/CGE using SDA technology (Figure 11 (b)) boosts di/dt , cutting E_{on} by 38%. These capacitance optimization techniques are applicable to both single IGBT and RC-IGBT structures.



D: Dummy Trench Gate;
A: Active Trench Gate

Figure 11: Schematic cross-sectional views of (a) Split gate (b) Split Dummy Active (right)

b) Thin Wafer Technology Using New Buffer layer

The most effective way to reduce conduction loss in IGBTs and free-wheeling diodes is to reduce the thickness of the wafer, however, this has the trade-off that the IGBT's SCSOA capability deteriorates. One way of adjusting the SCSOA is by lowering the concentration of the CS layer. Another indirect improvement effect on the SCSOA trade-off can be realized by a new buffer technology for Controlling charge-carrier Plasma Layer (CPL) developed mainly to suppress switching surges. CPL is a layer formed in the backside buffer region by a high-energy implantation of light elements and a low-temperature annealing process. By applying CPL, it is possible to suppress the increase in the electric field strength on the emitter side during SC operation particularly at room-temperature. By applying it to a CSTBT rated at 1200V/230A for instance, wafer thickness was reduced by approximately 10% while maintaining the SC capability, hence improving the conduction loss. In addition, the implementation of CPL solved the issue of the snap-off behavior during turn-off as it allows holes to remain in the backside prevent-

ing a rapid depletion of the carriers during surge voltage. Suppressing this phenomenon also enables reducing of wafer thickness.

c) RC-IGBT Chip Diode Placement Technology

In RC-IGBT, the IGBT and diode interfere with each other, so the boundary can cause an increase in on-state voltage, but since they also function as heat dissipation, the thermal resistance can be reduced and the power density can be increased compared to conventional methods. Since the IGBT's area is larger, the diodes are placed in within the area of the IGBT. The layout can be classified into stripe layout and island layout.

From a heat dissipation perspective, the island layout with a longer boundary length is advantageous. Accordingly, for the 3rd Generation RC-IGBT, a high-density island arrangement was developed to meet the stringent thermal management requirements of automotive applications. By increasing the diode density, heat dissipation efficiency was improved (T_j was reduced by 18%) and resulted in enhanced thermal distribution, effectively dispersing localized heat. The chip diode technology implemented in the 3rd Generation RC-IGBT also addresses snapback behavior in the I-V characteristics, ensuring a stable performance.

As shown in the experimental results in Figure 12, the device effectively mitigates excessive transient heat generated during IGBT short circuit testing. Furthermore, by finely arranging the Diode layout, the short-circuit withstand time is improved by 34% compared to the conventional stripe layout, demonstrating the superior thermal and electrical robustness of the technology.

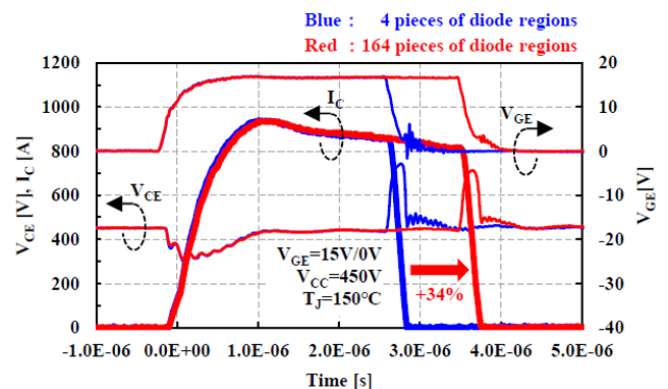


Figure 12: SCSOA of 3rd Gen. RC-IGBT with low and high density diode regions

d) Carrier Injection Diode Structure for RC-IGBT

To enhance RC-IGBT performance, a low-carrier injection diode structure was developed as demonstrated in Figure 13 to reduce recovery losses while maintaining ohmic contact. Key improvements include:

- Low-Concentration Anode Layer: The conventional anode layer is replaced with a lower-doped one, using a partial contact p+ layer to maintain good ohmic contact and suppress hole injection.
- Partial Cathode Layer: A selectively formed cathode layer (via precise photolithography process) limits carrier injection from the cathode while ensuring ohmic contact with the Al-based electrode. Optimizing the anode-cathode structure enables characteristic adjustment without lifetime control, achieving higher T_j by suppressing leakage current.
- Additionally, Local Lifetime Control: Proton implantation is applied to reduce carrier lifetime, further cutting tail current and switching losses in both the diode and IGBT regions.

These optimizations balance injection control and conductivity, enhancing efficiency and reducing losses in 3rd Gen. RC-IGBT.

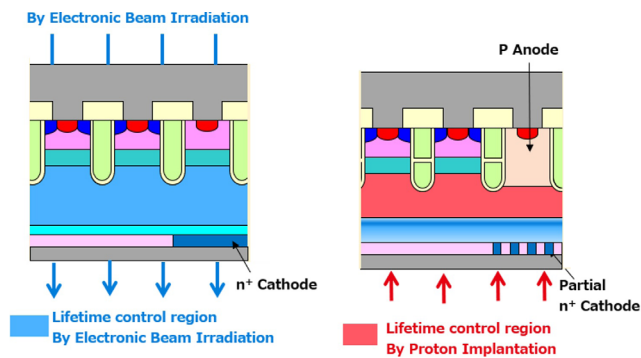


Figure 13: Schematic cross-sectional views of 2nd Gen. RC-IGBT (left) and 3rd Gen. RC-IGBT (right)

T_{vj} Simulation performance of RC-IGBT with J3 package

Despite the 3rd Generation RC-IGBT having a 22% smaller active area compared to the 7th Generation chipset, it achieves a 20% reduction in thermal resistance.

The current handling capability of the 3rd Gen. RC-IGBT was evaluated through simulations based on device characterization data and the resulted thermal resistance (see Figure 14). The simulation parameters were as follows: main battery voltage = 400 V, PWM switching frequency (f_{sw}) = 6, 8, and 10 kHz, coolant temperature (T_w) = 65°C, and coolant flow rate = 10 L/min. Under 8 kHz switching, the inverter output current exceeds 250 Arms, while maintaining a maximum junction temperature below 175°C. Compared to the 7th Generation IGBT chipset, the 3rd Gen. RC-IGBT demonstrates improved performance.

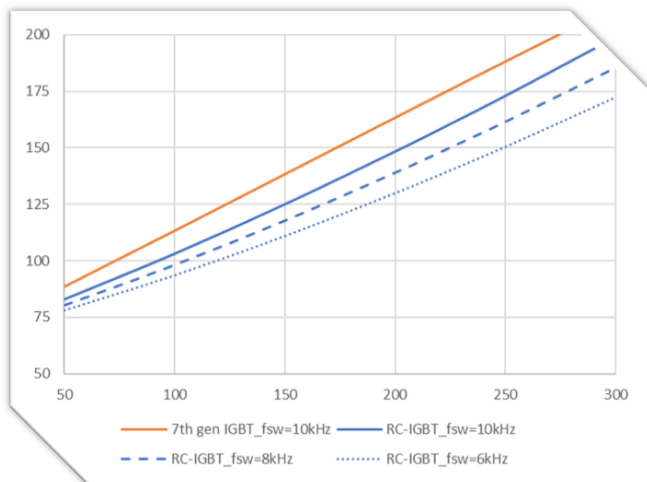


Figure 14: T_{vj} simulation of J3 based RC-IGBT

Closing Remarks

Mitsubishi Electric is steadily moving forward in advancing its next generation of innovative efficient semiconductor bare-dies (SiC MOSFET & Si RC-IGBT) and compact high-reliability transfer mold packaging (T-PM) towards scalable, cost-effective, and reliable e-Mobility solutions.

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