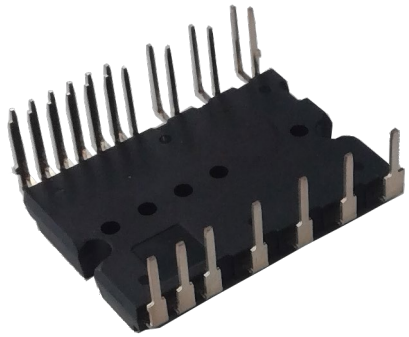
MITSUBISHI ELECTRIC

< DIPIPM >

PSS50SF1F6

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



MAIN FUNCTION AND RATINGS

- Inverter bridge for three phase DC-to-AC power conversion
- 600V / 50A
- TRANSFER MOLDING TYPE
- Open emitter type
- Built-in bootstrap diodes with current limiting resistor

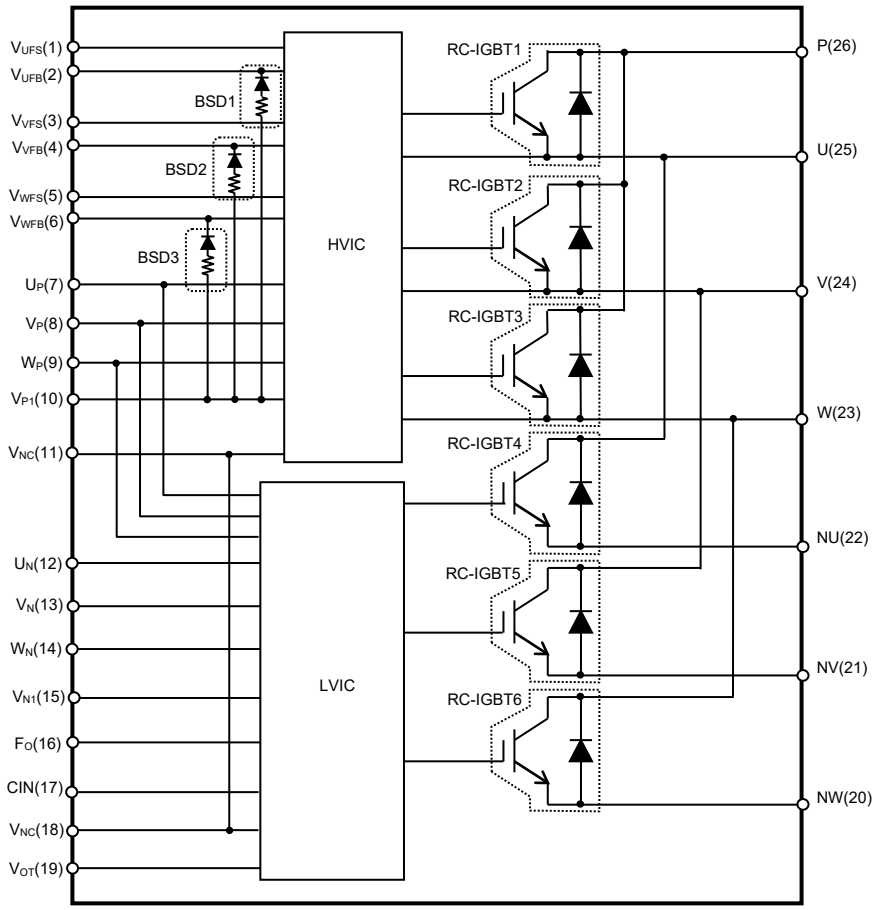
APPLICATION

- AC 100~240Vrms(DC voltage:400V or below) class low power motor control

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage protection (UV)
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC)
- Fault signaling : Corresponding to SC fault (N-side RC-IGBT) and UV fault (N-side supply)
- Temperature output : Outputting LVIC temperature by analog signal
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V
V_{CES}	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	T_C=25°C (Note 1)	50	A
$\pm I_{CP}$	Each IGBT collector current (peak)	Tc=25°C, less than 1ms, non-repetitive	100	A
T_{jop}	Junction temperature	Continuous operation (Note 2)	-40～+150	°C
T_{jmax}	Junction temperature	Temporally operation (e.g. overload)	175	°C

(Note1) Pulse width and period are limited due to junction temperature.
(Note2) The maximum junction temperature rating of built-in power chips is 175°C(@Tc≤125°C).However, to ensure safe operation of DIPIPM, the average junction temperature should be limited to Tj≤150°C (@Tc≤125°C).

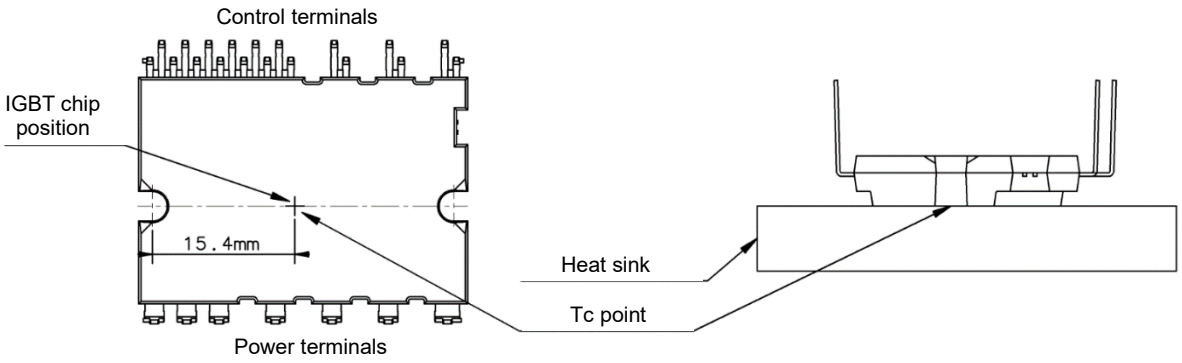
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between	20	V
V_{DB}	Control supply voltage	Applied between	20	V
V_{IN}	Input voltage	Applied between	-0.5～V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between	-0.5～V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	5	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5～V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part T_j = 150°C, less than 2μs, non-repetitive	400	V
T_C	Module case operation temperature	Measurement point of Tc is described in Fig.1	-40～+125	°C
T_{stg}	Storage temperature		-40～+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	Vrms

Fig. 1 T_C MEASUREMENT POINT



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 3)	Inverter RC-IGBT part (per 1/6 module)	-	-	0.85	K/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.4K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m•K).

ELECTRICAL CHARACTERISTICS (T_{ch} = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D = V_{DB} = 15V, V_{IN} = 5V, I_C = 50A	-	1.37	1.67	V
V_{EC}	FWDi forward voltage	V_{IN} = 0V, -I_C = 50A	-	1.43	1.76	V
t_{on}	Switching times	V_{CC}= 300V, V_D= V_{DB}= 15V I_C= 50A, T_j= 25°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)	0.65	1.05	1.49	μs
t_{rr}			-	0.21	-	μs
$t_{c(on)}$			-	0.36	0.65	μs
t_{off}			-	1.20	1.64	μs
$t_{c(off)}$			-	0.16	0.37	μs
I_{CES}	Collector-emitter cut-off current	V_{CE}=V_{CES}	-	-	1	mA

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	4.00	mA
			V_D=15V, V_{IN}=5V	-	-	4.00	
I_{DB}		Each part of V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	V_D=V_{DB}=15V, V_{IN}=0V	-	-	0.55	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	0.55	
$V_{SC(ref)}$	Short circuit trip level	V_D = 15V (Note 4)		0.455	0.480	0.505	V
UV_{DBt}	P-side Control supply under-voltage protection(UV)	Trip level		10.2	-	12.9	V
UV_{DBr}		Reset level		10.2	-	12.9	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)	Trip level		10.3	-	12.5	V
UV_{Dr}		Reset level		10.8	-	13.0	V
V_{OT}	Temperature Output	Pull down R=5.1kΩ (Note 5)	LVIC Temperature=90°C	2.63	2.80	2.97	V
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA			-	0.95	V
t_{FO}	Fault output pulse width	(Note 6)		200	-	-	μs
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	2.20	2.60	V
$V_{th(off)}$	OFF threshold voltage			0.80	1.40	-	V
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.35	0.80	-	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor (Note 7)		0.5	0.9	1.3	V
R	Built-in limiting resistance	I_F=300mA		16	20	24	Ω

Note 4 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than Icp.

5 : For temperature output type, DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM. Temperature of LVIC vs. VOT output characteristics is described in Fig. 3.

6 : Fault signal Fo outputs when SC or UV protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 200μs), but at UV failure, Fo outputs continuously until recovering from UV state. (But minimum Fo pulse width is 200μs.)

7 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of Bootstrap Di V_F-I_F curve (@Ta=25°C) Including Voltage Drop by Limiting Resistor (Right chart is enlarged chart.)

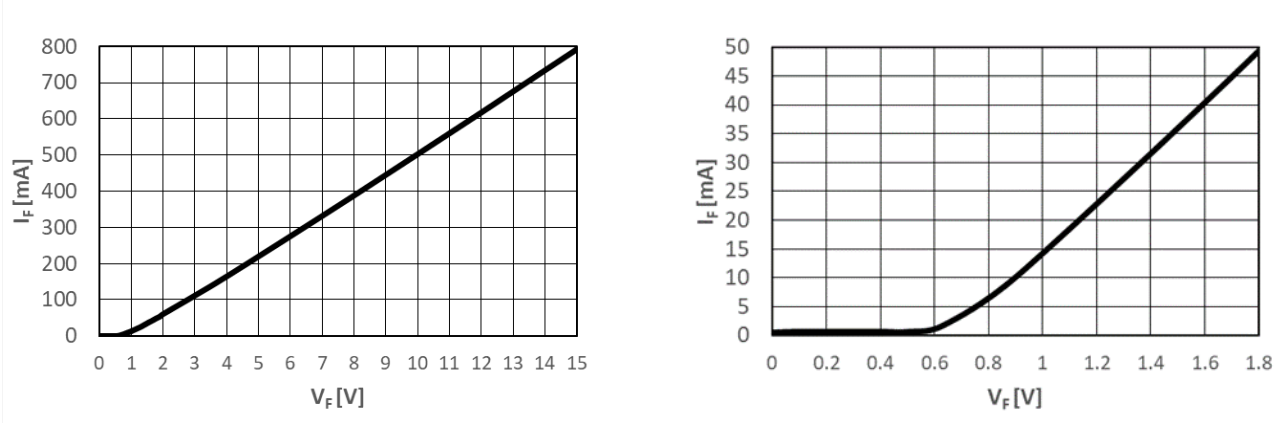


Fig. 3 Temperature of LVIC vs. VOT Output Characteristics

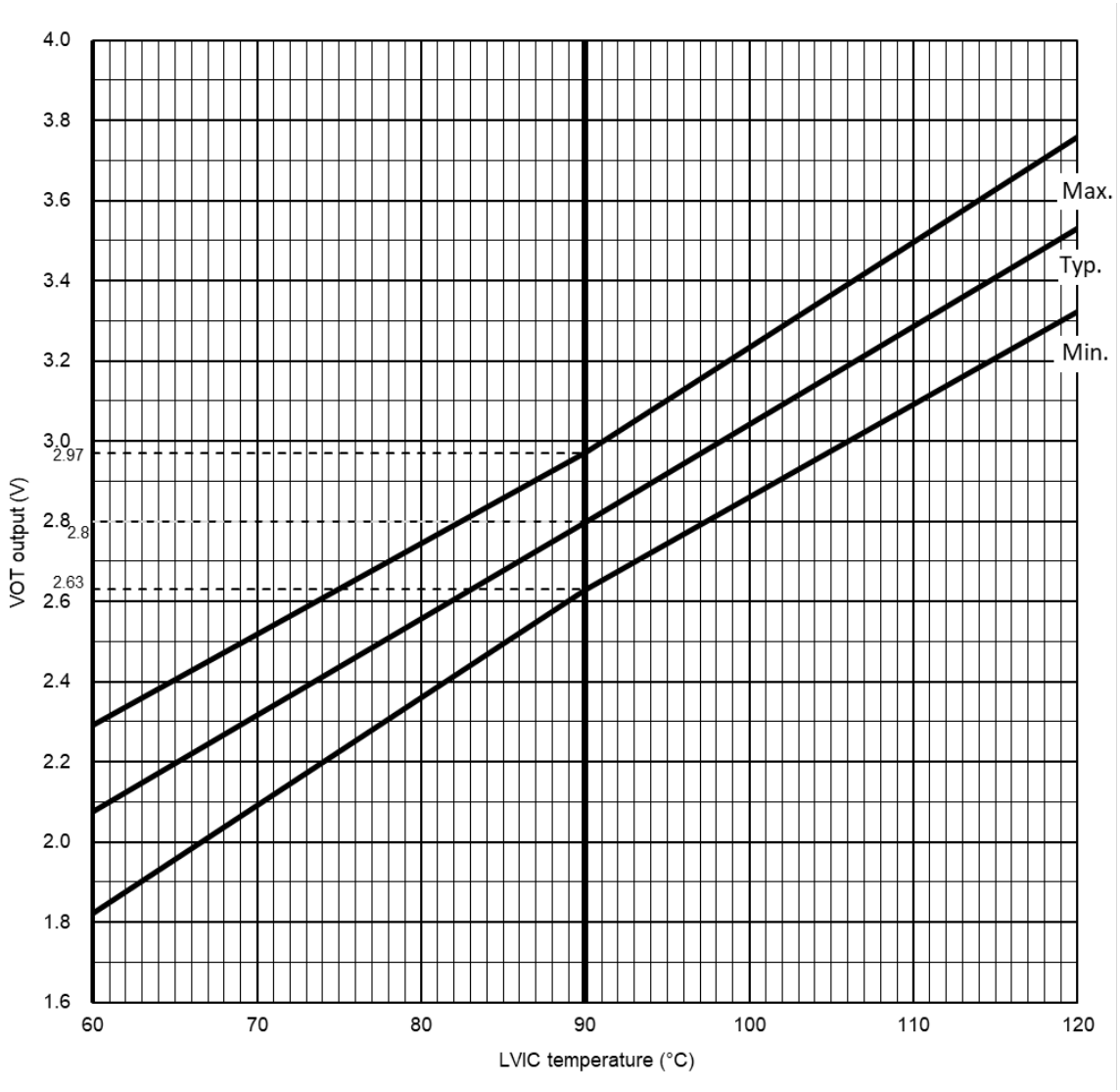
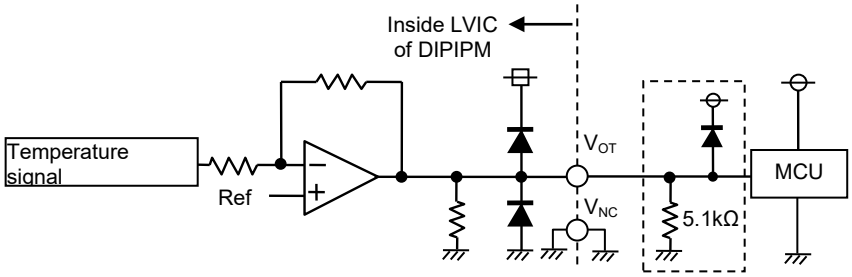


Fig. 4 VOT output circuit



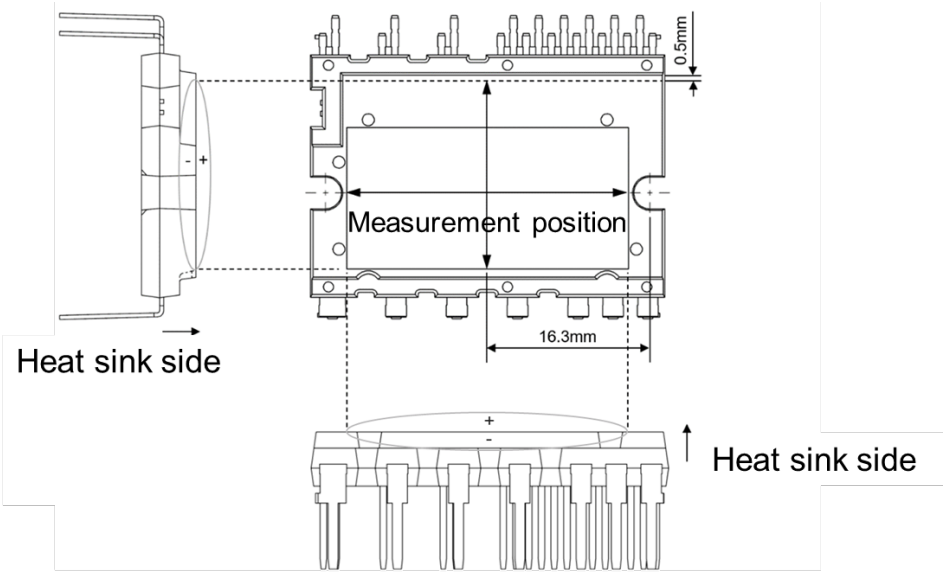
(1) It is recommended to insert 5kΩ (5.1kΩ is recommended) pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC}(control GND), the extra circuit current, which is calculated approximately by V_{OT} output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V_{OT} for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.

(2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and V_{OT} output for preventing over voltage destruction.

(3) In the case of not using V_{OT}, leave V_{OT} output NC (No Connection).
Refer the application note about the usage of V_{OT}.

Parameter	Condition	Reference	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 8)	JEITA-ED-4701 402 method Ⅱ	0.59	0.69	0.78	N·m
Terminal pulling strength	Control terminal: Load 2.3N Power terminal: Load 2.3N	JEITA-ED-4701 401 method Ⅰ	30	-	-	s
Terminal bending strength	15deg. Bend	JEITA-ED-4701 401 method Ⅲ	1	-	-	times
Weight		-	-	10.3	-	g
Heat radiation part flatness	(Note 9)	-	-30	-	+100	μm

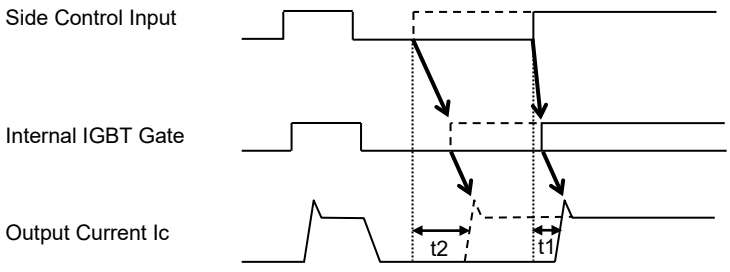
Note 8: Plain washers (JIS B1256) are recommended.
Note 9: Measurement point of heat radiation part flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	P-NU, NV, NW 端子間	0	300	400	V
V_D	Control supply voltage	V_{P1}-V_{NC}, V_{N1}-V_{NC} 端子間	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}端子間	13.0	15.0	18.5	V
ΔV_D,ΔV_{DB}	Control supply variation		-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal	2.0	-	-	μs
f_{PWM}	PWM input frequency	T_C≦ 125℃, T_j≦ 150℃	-	-	20	kHz
PWIN(on)	Minimum input pulse width	(Note10)	0.7	-	-	μs
PWIN(off)		(Note11)	1.5	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)	-5.0	-	+5.0	V

Note10: DIPIPM might not make response if the input signal pulse width is less than PWIN(on).
Note11: DIPIPM might make no response or delayed response (P-side IGBT only) for input pulse width less than PWIN(off). Over rated collector current (Ic) operation, DIPIPM might make delayed response even if the input signal pulse width is PWIN(off) or more.
The timing charts are described as below.

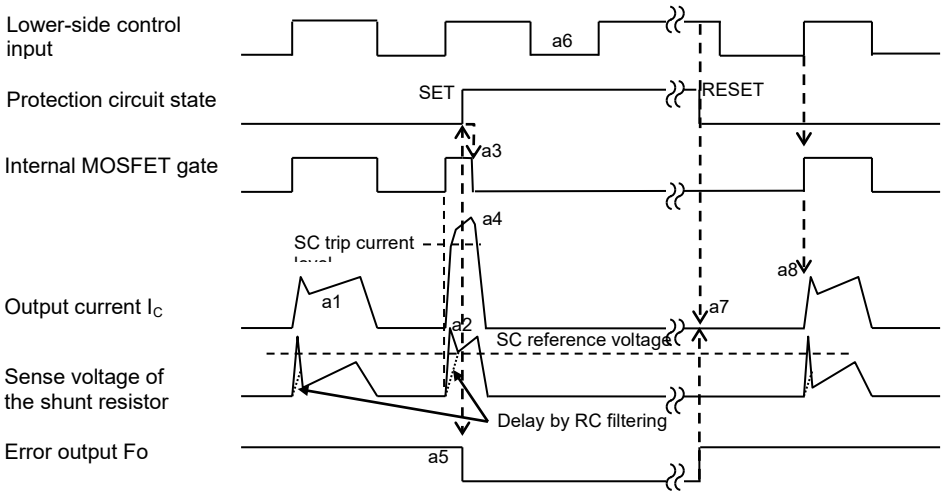


Real line: Normal response; turn on time t1
Broken line: Delayed response; turn on time t2
(t1: Normal switching time)

Fig. 5 Timing Charts of The DIPIPM Protective Functions

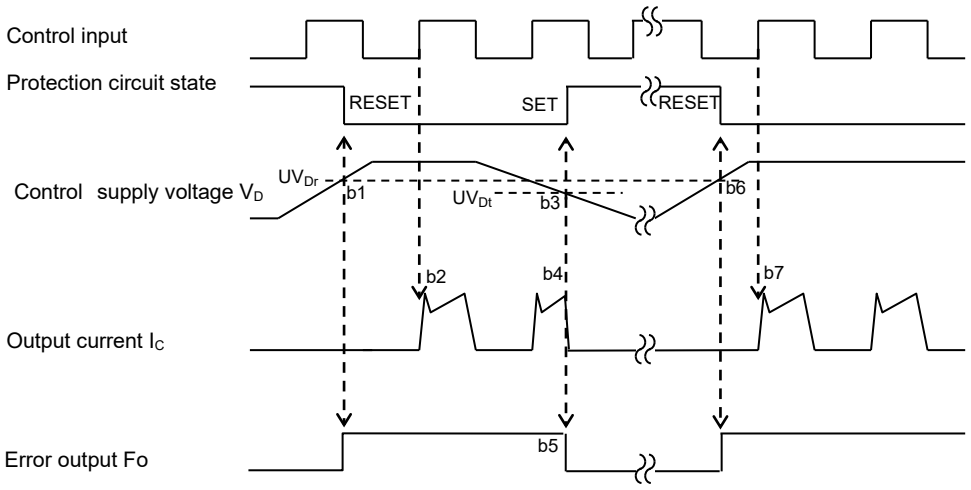
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: MOSFET ON and outputs current.
a2. Short circuit current detection (SC trigger)
(It is recommended to set RC time constant 1.5~2.0μs so that MOSFET shut down within 2.0μs when SC.)
a3. All N-side MOSFETs gates are hard interrupted.
a4. All N-side MOSFETs turn OFF.
a5. F_O outputs for t_{Fo}=minimum 200μs.
a6. Input = "L": MOSFET OFF
a7. Fo finishes output, but MOSFETs don't turn on until inputting next ON signal (L→H).
(MOSFETs of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: MOSFET ON and outputs current.



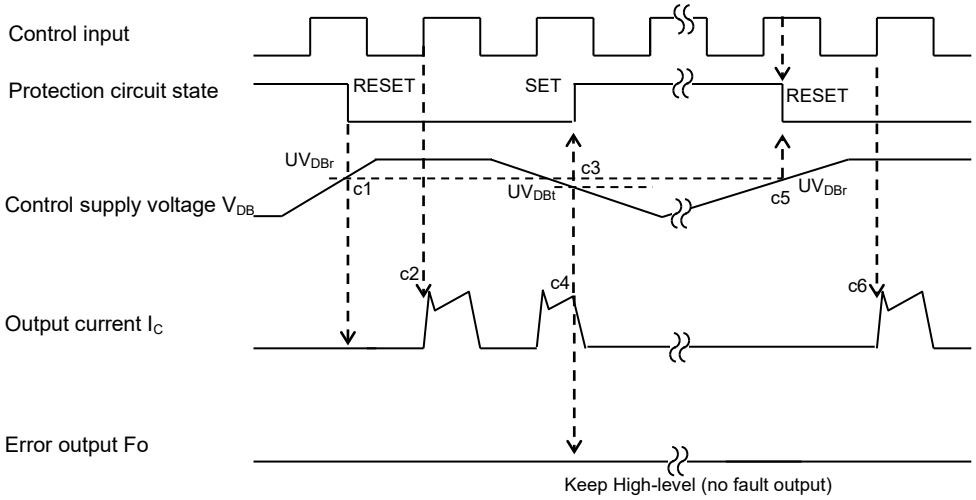
[B] Under-Voltage Protection (N-side, UV_D)

b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but MOSFET turns ON by next ON signal (L→H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)
b2. Normal operation: MOSFET ON and outputs current.
b3. V_D level drops to under voltage trip level. (UV_{Dt}).
b4. All N-side MOSFETs turn OFF in spite of control input condition.
b5. Fo outputs for t_{Fo}=minimum 200μs, but output is extended during V_D keeps below UV_{Dr}.
b6. V_D level reaches UV_{Dr}.
b7. Normal operation: MOSFET ON and outputs current.



[C] Under-Voltage Protection (P-side, UV_{DB})

c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, MOSFET turns on by next ON signal (L→H).
c2. Normal operation: MOSFET ON and outputs current.
c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
c4. MOSFET of the corresponding phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
c5. V_{DB} level reaches UV_{DBr}.
c6. Normal operation: MOSFET ON and outputs current.



[D] Interlock Sequence

d1. When N-side is ON state(H), P-side turn ON(L→H) ····· N-side shut off(Note12)
d2. When P-side is ON state(H), N-side turn ON(L→H) ····· N-side shut off
d3. P-side turn OFF(H→L) and N-side is ON state(H) ····· N-side turn ON(Note12)
(Note12) When d1 and d3 are active, a small-time-period through current may flow due to the difference in transmission delay between the control inputs on the P-side and N-side and the internal IGBT gate signal.

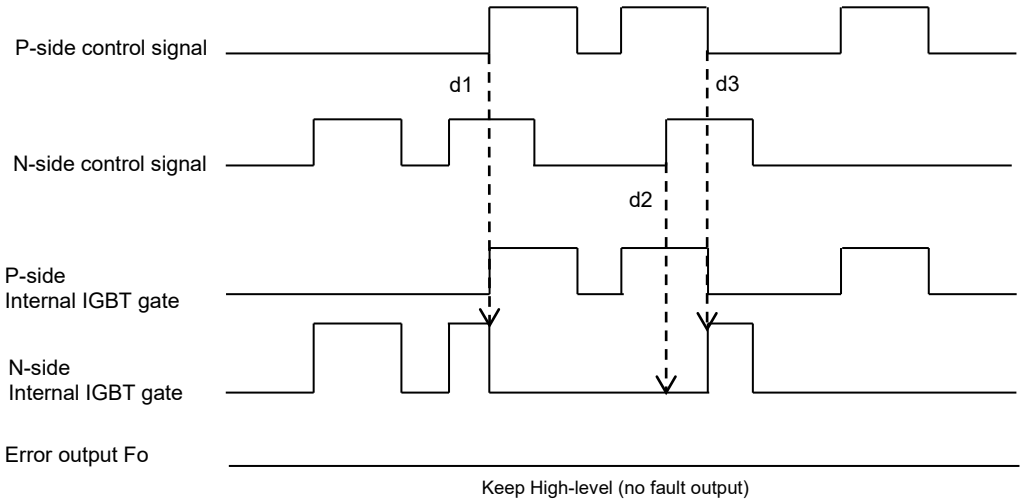
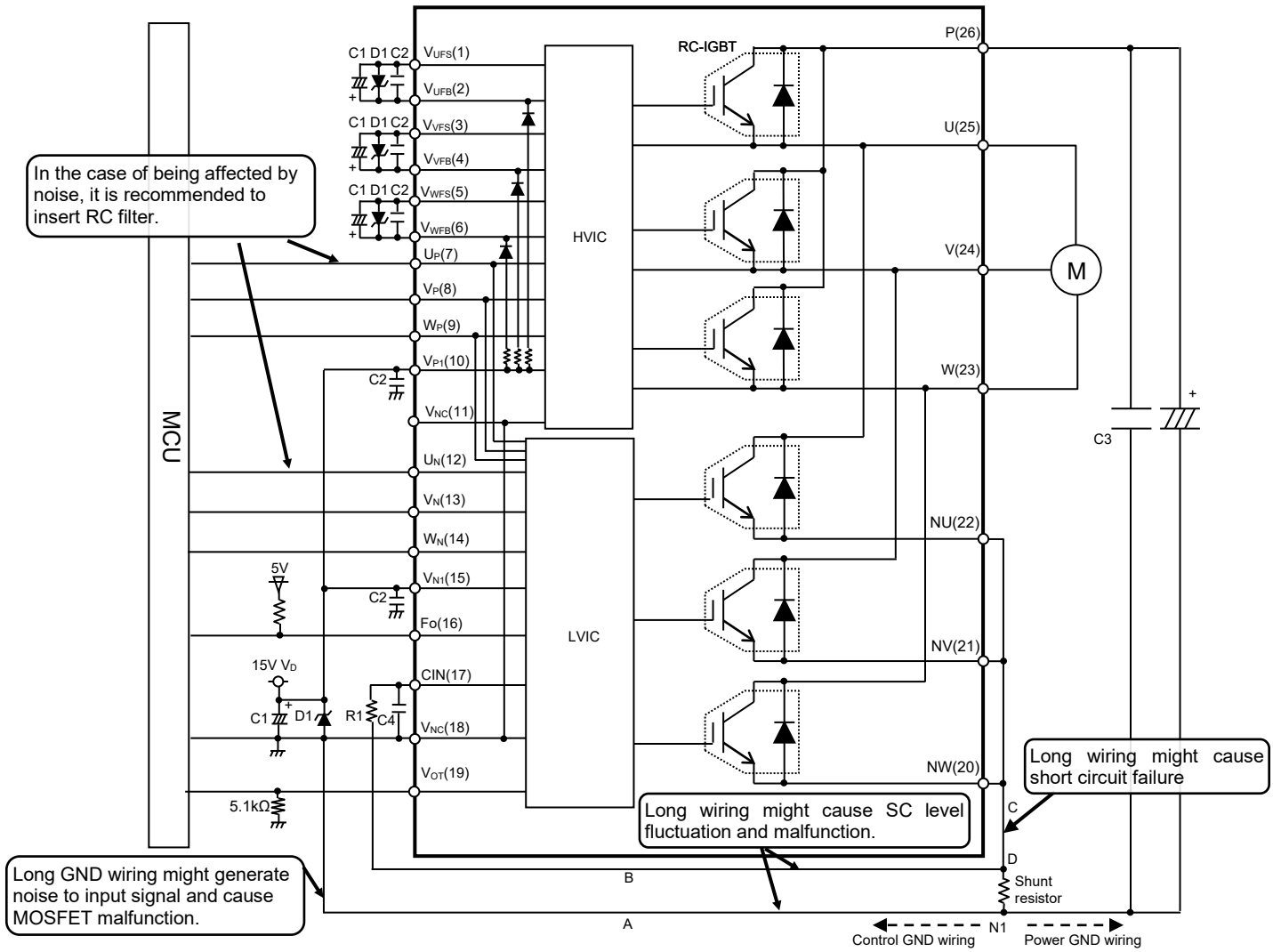
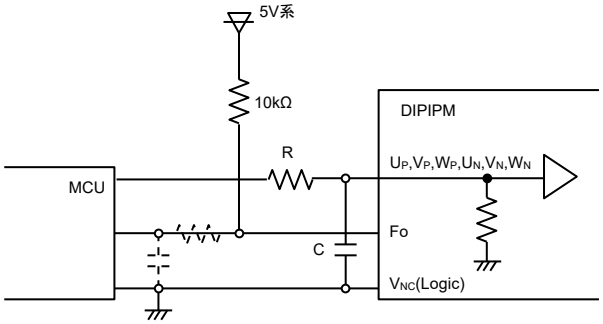


Fig. 6 Example of Application Circuit



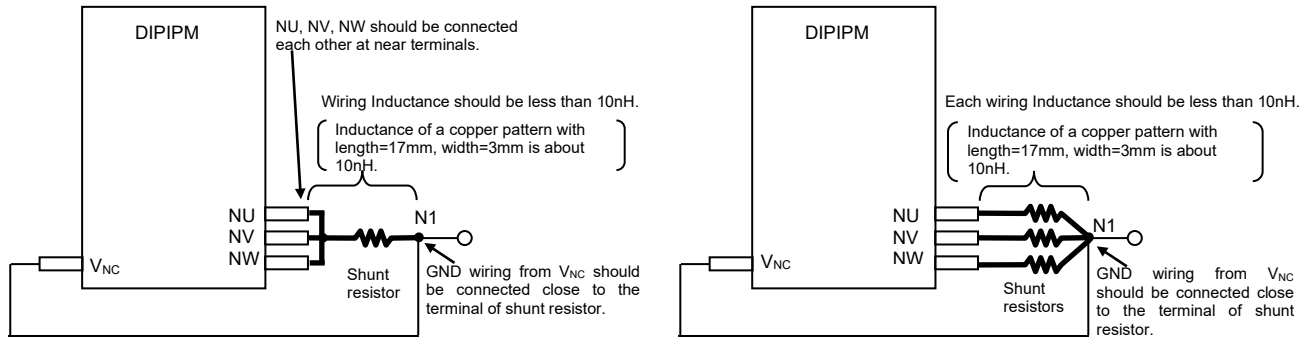
(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
(2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.
(3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a snubber capacitor C3 (more than 0.1μF) between the P-N1 terminals is recommended. C3 capacitor value should be selected by enough system evaluation.
(4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
(5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals.
(7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2: 0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
(8) Input drive is High-active type. There is a minimum 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
(9) Thanks to built-in HVIC, direct coupling to MCU without any optocoupler or transformer isolation is possible.
(10) Fo output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes IFo up to 1mA. (IFO is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.)
(11) Two VNC terminals are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.
(12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.
(13) For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase MOSFET or other DIPIPM.

Fig. 7 MCU I/O Interface Circuit



Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.
The DIPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

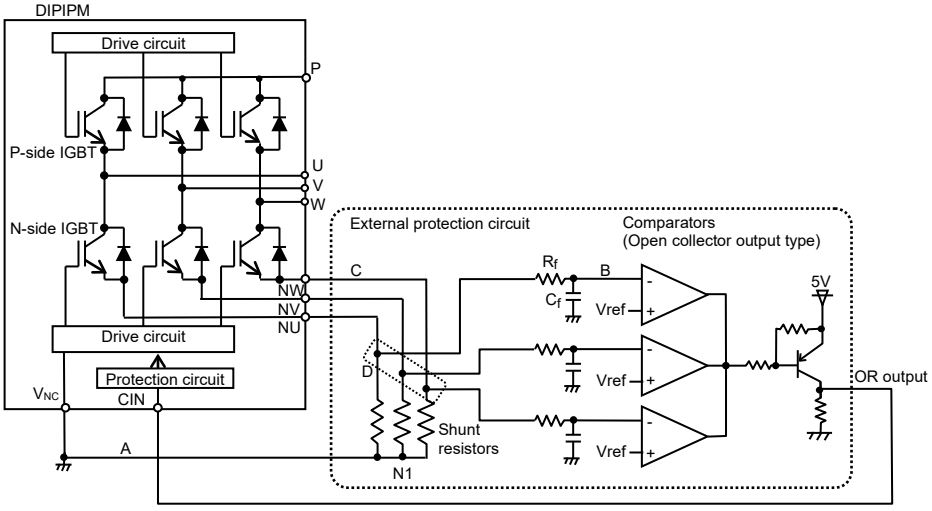
Fig. 8 Pattern Wiring Around the Shunt Resistor



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

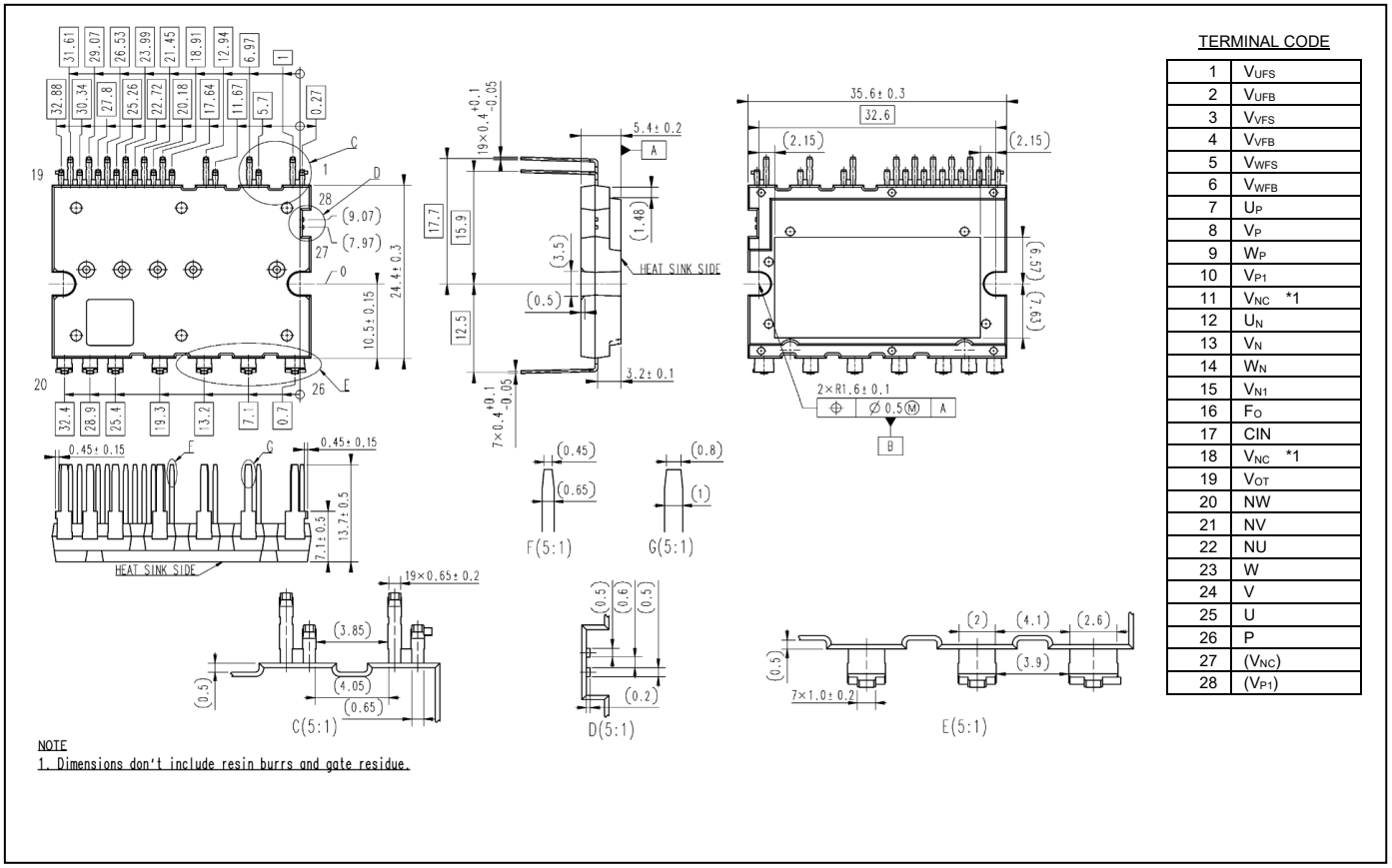
Fig. 9 External SC Protection Circuit with Using Three Shunt Resistors

When DIPIPM is operated with three shunt resistors, voltage of each shunt resistor cannot be input to CIN terminal directly. In that case, it is necessary to use the external protection circuit as below.



(1) It is necessary to set the time constant R_fC_f of external comparator input so that MOSFET stop within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(2) The threshold voltage Vref should be set up the same rating of short circuit trip level (Vsc(ref) typ. 0.48V).
(3) Select the external shunt resistance so that SC trip-level is less than specified maximum value.
(4) To avoid malfunction, the wiring A, B, C should be as short as possible.
(5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
(6) OR output high level should be over 0.505V (=maximum Vsc(ref)).
(7) GND of Comparator, Vref circuit and Cf should be not connected to noisy power GND but to control GND wiring.

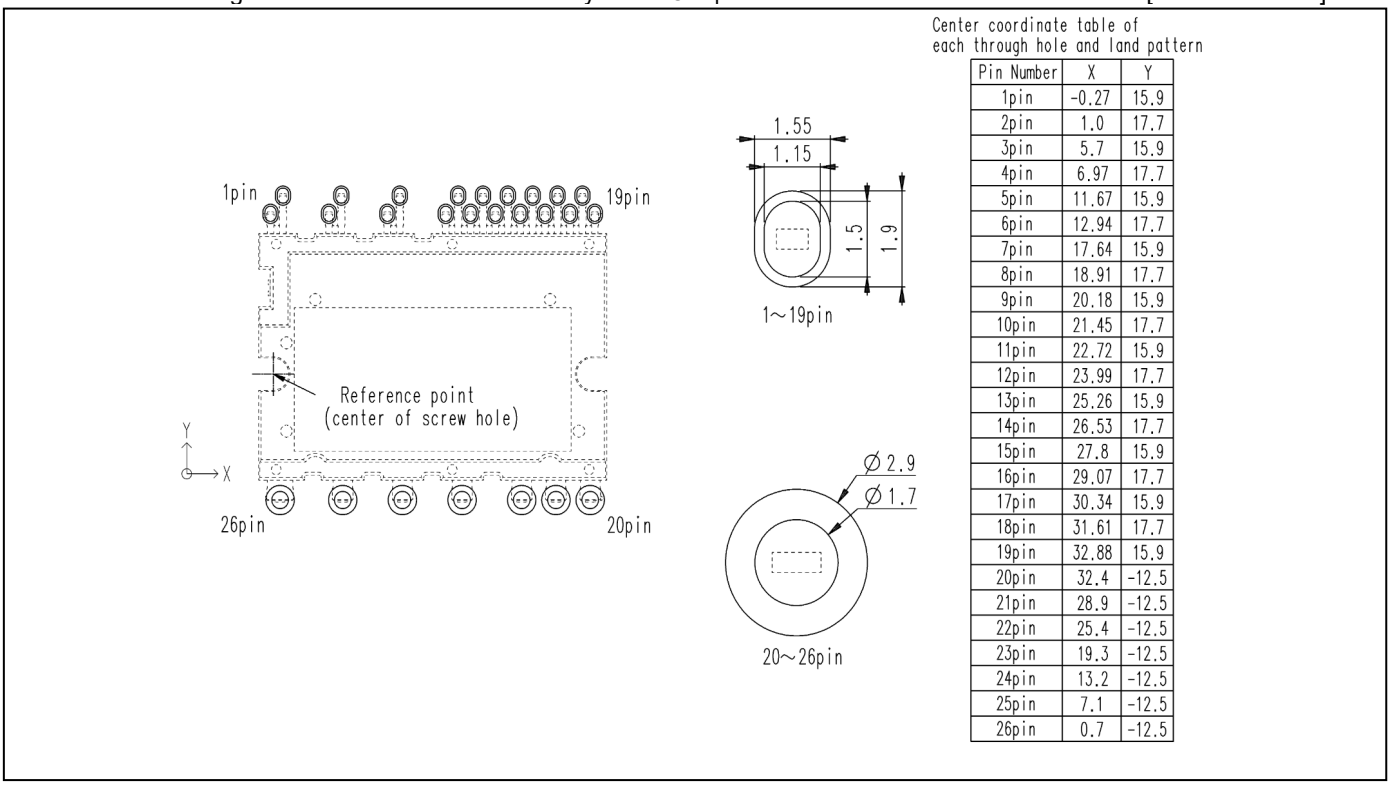
Fig. 10 Package Outlines [Dimension: mm]



TERMINAL CODE

1	V_{UFS}
2	V_{UFB}
3	V_{VFS}
4	V_{VFB}
5	V_{WFS}
6	V_{WFB}
7	U_P
8	V_P
9	W_P
10	V_{P1}
11	V_{NC} *1
12	U_N
13	V_N
14	W_N
15	V_{N1}
16	F_O
17	CIN
18	V_{NC} *1
19	V_{OT}
20	NW
21	NV
22	NU
23	W
24	V
25	U
26	P
27	(V_{NC})
28	(V_{P1})

Fig. 11 (Reference Figure) PCB Through-hole Pattern
Recommended through-hole locations and diameter layout for Compact DIPIPM [Dimension: mm]



Center coordinate table of each through hole and land pattern

Pin Number	X	Y
1pin	-0.27	15.9
2pin	1.0	17.7
3pin	5.7	15.9
4pin	6.97	17.7
5pin	11.67	15.9
6pin	12.94	17.7
7pin	17.64	15.9
8pin	18.91	17.7
9pin	20.18	15.9
10pin	21.45	17.7
11pin	22.72	15.9
12pin	23.99	17.7
13pin	25.26	15.9
14pin	26.53	17.7
15pin	27.8	15.9
16pin	29.07	17.7
17pin	30.34	15.9
18pin	31.61	17.7
19pin	32.88	15.9
20pin	32.4	-12.5
21pin	28.9	-12.5
22pin	25.4	-12.5
23pin	19.3	-12.5
24pin	13.2	-12.5
25pin	7.1	-12.5
26pin	0.7	-12.5

1) Pins 11 and 18 of the VNC (control power GND terminal) are internally connected. Use only one pin; leave the other pin in the NC (no connection) state.

Important Notice

The information contained in this datasheet shall in no event be regarded as a guarantee of conditions or characteristics. This product has to be used within its specified maximum ratings, and is subject to customer's compliance with any applicable legal requirement, norms and standards.

Except as otherwise explicitly approved by Mitsubishi Electric Corporation in a written document signed by authorized representatives of Mitsubishi Electric Corporation, our products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

In usage of power semiconductor, there is always the possibility that trouble may occur with them by the reliability lifetime such as Power Cycle, Thermal Cycle or others, or when used under special circumstances (e.g. condensation, high humidity, dusty, salty, highlands, environment with lots of organic matter / corrosive gas / explosive gas, or situations which terminals of semiconductor products receive strong mechanical stress). Therefore, please pay sufficient attention to such circumstances. Further, depending on the technical requirements, our semiconductor products may contain environmental regulation substances, etc. If there is necessity of detailed confirmation, please contact our nearest sales branch or distributor.

The contents or data contained in this datasheet are exclusively intended for technically trained staff. Customer's technical departments should take responsibility to evaluate the suitability of Mitsubishi Electric Corporation product for the intended application and the completeness of the product data with respect to such application. In the customer's research and development, please evaluate it not only with a single semiconductor product but also in the entire system, and judge whether it's applicable. As required, pay close attention to the safety design by installing appropriate fuse or circuit breaker between a power supply and semiconductor products to prevent secondary damage. Please also pay attention to the application note and the related technical information.

Keep safety first in your circuit designs!

Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

- These materials are intended as a reference to assist our customers in the selection of the Mitsubishi Electric Semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.
- Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
- All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Electric Semiconductor product distributor for the latest product information before purchasing a product listed herein. The information described here may contain technical inaccuracies or typographical errors. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
  Please also pay attention to information published by Mitsubishi Electric Corporation by various means, including the Mitsubishi Electric Semiconductor home page (http://www.MitsubishiElectric.com/semiconductors/).
- When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
- Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Electric Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
- The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.
- If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
  Any diversion or re-export contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
- Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Electric Semiconductor product distributor for further details on these materials or the products contained therein.